Open Defect Detection of Multiple Function Gates by Impedance Analysis

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**Abstract.** A SoC (System-on-a-Chip) integrates almost all required component electronic circuits for a fully functional system into a single silicon chip on a single IC (*Integrated Circuit*). One of the components contains is a CPU (Central Processing Unit). In the CPU, at least the main component is ALU (Arithmetic Logic Unit) in which it performs basic arithmetic operations and logical operations. One of the ALU operations is 2-input NAND gate of a multiple function gate. However, an open defect may occur at an interconnect inside it. In this paper, an impedance analysis is proposed to detect the open defect inside the function gate. The function gate is designed and simulated by SPICE (Simulation Program with Integrated Circuit Emphasis) and LTspice XVII, respectively. The analysis is plotted in a Bode plot. Furthermore, the analysisresult shows that magnitude and phase signals of the defective IC decrease linearly with increasing sizes of the defect.

**Keywords:** Open defect, multiple function gate, impedance analysis

# INTRODUCTION

In the last few years, an EMIB (Embedded Multi-die Interconnect Bridge) provides unique packaging paradigm of very high density interconnects to connect multiple chips in a single package[1]. The EMIB simplifies the design process and offers flexibility.

A SoC (System-on-a-Chip) integrates almost all required component electronic circuits for a fully functional system into a single silicon chip on a single IC (Integrated Circuit)[2]. The components usually contain a CPU (Central Processing Unit), a GPU (Graphics Processing Unit), memory, USB (Universal Serial Bus) controller, power management circuits, and wireless radios. Because the SoC includes both the hardware and software, it uses less power, has better performance, requires less space and is more reliable than multichip systems.

A CPU is a complex electronic circuit that comprises several key components that process data and run instructions[3]. The main components of a CPU are control unit, registers, ALU (Arithmetic Logic Unit), memory management unit, and clock.

The ALU performs basic arithmetic operations (addition, subtraction, multiplication, and division) and logical operations (AND, OR, and NOT) on data[4]. It receives data from registers within the CPU, processes it based on the instructions from the control unit, and produces the result.

One of the ALU operation example is a multiple function gate[5]. It is a configurable multiple function gate with 3-bit inputs. It provides the flexibility to implement various logic functions with a reduced pin count. Moreover, it can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer. Furthermore, it is composed by NOR, 2 NAND, and 3 inverter gates.

An open defect may occur at an interconnect between logic gates inside the IC during a fabrication process[6]. Since the interconnect in the IC layout made by a metal, the defect may be caused the open metal. Thus, the metal may be modeled by a resistance, since the defect related to the resistance value.

Fault tolerant approaches have been applicated to detect the defect[7]. The approaches mean the ability of the SoC to maintain functionality, reliability, and performance in the presence of the defect. However, the approaches require additional resources and expenditure to test and monitor the defect since they do not generate automatically results.

There are many DfT (Design for Testability) have been proposed to detect the defect[8]. The DfT added the designed IC by testability features such as scan chain, BIST (Built-in Self Test), and Boundary Scan Cell. The added features easier to test during the manufacturing and debugging process. Nevertheless, it takes long test time and also effort necessary to generate test vector sequences.

Deep learnings have been proposed into the IC design to reduce the chip development time and increase powerful performance[9]. In addition, the learnings applied to optimize the design of its location and shape. But, the learnings limited their ability to generalize to new predictions without training the previous data.

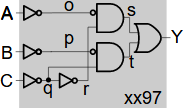
A FFT (Fast Fourier Transform) analysis has been proposed to detect the open defect[10]. Although the IC operated in a high speed time, it is easier to be analyzed by the FFT operating in a frequency domain signal. However, the FFT has the limited frequency domain. It means that the FFT may not accurately distinguish closely spaced frequency components.

In this paper, the open defect inside the multiple function gate of an IC may be detected by proposing an impedance analysis. The IC is adapted by a SPICE (Simulation Program with Integrated Circuit Emphasis) netlist library designed by Nexperia Co. Ltd[11]. Then, it is simulated using LTspice XVII produced by Analog Devices Inc[12]. The analysis is facilitated by menu of the LTspice and generated of the IC in an impedance domain signal. The analysis result shows that magnitude and phase signals of the defective IC decrease linearly with increasing sizes of the defect.

# METHODS

A functional diagram of a configurable multiple function gate is shown in **FIGURE 1**. There are 3 input pins of the function gate, i.e., A, B, and C nodes, and 1 output pin, i.e., Y node. The function gate may be selected in 6 logic functions, e.g., 2-input MUX, 2-input AND, 2-input OR with one input inverted, 2-input NAND with one input inverted, 2-input AND with one input inverted, 2-input NOR with one input inverted, 2-input OR, inverter, and buffer.

An open defect may occur at one of interconnects between logic gates inside the function gate, i.e., o, p, q, r, s, and t nodes. The defect related to resistance values in which the values are generalized by impedances. The impedance is a measure of dividing between generated AC voltage signals and flowed currents. Thus, an impedance analysis is proposed to detect the defect by providing an AC voltage signal to the input pins and measuring impedance response signals in the output pin. The response signals are determined by Equation 1. Then, the impedance analysis results are plotted in a Bode plot. It is a waveform viewer of magnitude and phase over frequency in which the magnitude may be selected in a linear scaling representation.

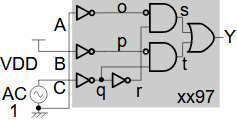


**FIGURE 1**. A Configurable Multiple Function Gate

(1)

# RESULTS AND DISCUSSION

An open defect at an interconnect inside 2-input NAND function gate is selected to be detected by proposing an impedance analysis. A functional diagram of the NAND gate is shown in **FIGURE 2**. It based on a SPICE netlist library designed by Nexperia Co. Ltd. Furthermore, it is simulated using the free SPICE simulator of LTspiceXVII produced by Analog Devices Inc.

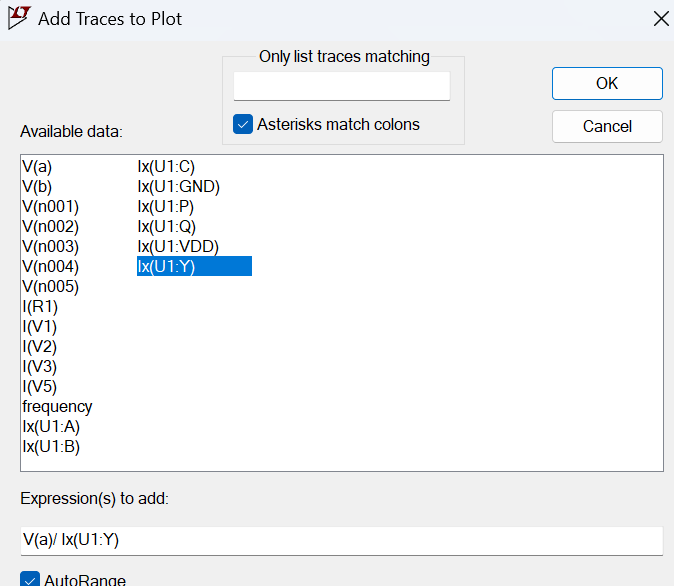


**FIGURE 2**. 2-input NAND Function Gate

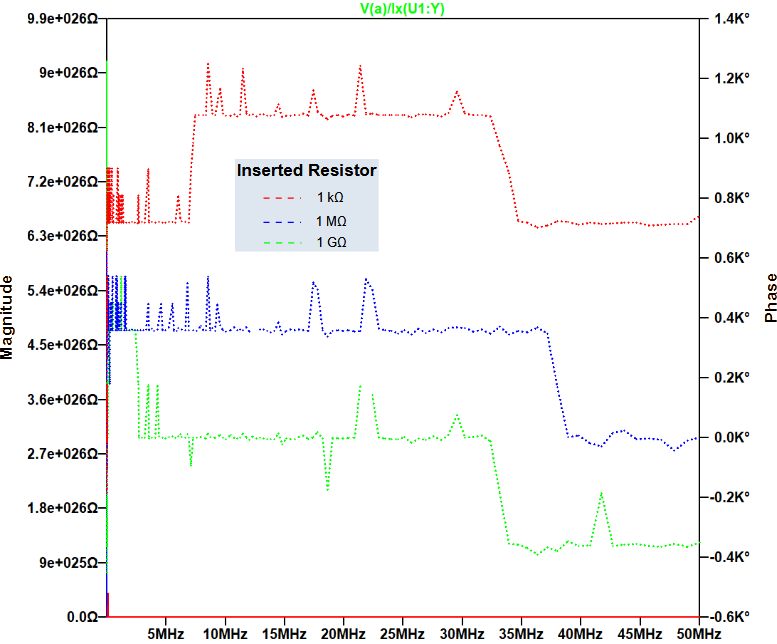
The o node of the NAND gate became a targeted open defect and inserted by resistors of 1 kΩ, 1 MΩ, 1 GΩ. The C input pin is provided by an AC voltage signal of an amplitude 1 V. The A and B input pins are connected to ground and 3V VDD, respectively. An AC Analysis command of the LTspiceXVII is provided, i.e., sweep type of decade, point per decade of 100, start frequency of 10 Hz, and stop frequency of 50 MHz.

Measuring the response signals of the Y output pin is determined by Equation 1 and displayed by the LTspiceXVII as shown in **FIGURE 3**. Moreover, the impedance analysis result is plotted by a waveform viewer as magnitude and phase over frequency of a Bodde plot. A linear scaling representation is selected by the magnitude of the plot. The analysis result is shown in **FIGURE 4**.

As shown in Figure 4, impedances of the defective NAND function gate decrease linearly with increasing the inserted resistors. It means that the measured impedances are related to sizes of the defect. Specifically, larger the sizes of the defect correlated with decreasing the measured impedances.



**FIGURE 3**. 2-input NAND Function Gate



**FIGURE 4**. Impedance analysis result

# CONCLUSIONS

2-input NAND of a configurable multiple function gate is selected to be detected of an open defect at an interconnect inside it by proposing an impedance analysis. Resistors of 1 kΩ, 1 MΩ, 1 GΩ are inserted to the targeted open defect. Furthermore, designing the NAND gate is adapted by SPICE netlist library. The impedance analysis result of the function gate is derived by simulating it in LTspiceXVII. Impedances of the defective NAND gate decrease linearly with increasing the inserted resistors or sizes of the defect.

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