Open Defect Detection inside Logic ICs by Laplace Transform

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**Abstract.** A logic IC (*Integrated Circuit*) is often used within an embedded system which it is a computer system designed to perform a specific task within a larger mechanical or electrical system.   
Moreover, the embedded system may integrate the logic IC with microcontrollers or FPGAs (*Field Programmable Logic Arrays*) to handle real-time tasks or speed-critical operations. Unfortunately, an open defect may occur at interconnects between gates inside the logic IC. In this paper, a Laplace transform is proposed to detect an open defect inside a logic IC. The IC is designed in a SPICE (Simulation Program with Integrated Circuit Emphasis) netlist library. Moreover, it is simulated using LTspice XVII. The LTspice has available menu to implement the Laplace transform syntax. Bothmagnitudes and phases of the Laplace output decrease linearly with increasing the defect.

**Keywords:** Open defect, logic IC, Laplace transform

# INTRODUCTION

A logic IC (*Integrated Circuit*) is a type of semiconductor devices using logic gates, combinational logic gates, and sequential logic gates implemented in digital logic functions[1]. The gates are fundamental building blocks, i.e., NOT, Multiplexers, Flip-flops, etc. The IC is often used within an embedded system.

The embedded system is a computer system designed to perform a specific task within a larger mechanical or electrical system[2]. It has some hardware components, e.g., microcontroller / microprocessor, memory, input/output interfaces. It has characteristics like real-time operation, resource-constrained, low power consumption, and application-specific.

Furthermore, the embedded system often used the logic ICs to handle tasks, for example: signal routing, timing, or implementing custom hardware logic[3]. Moreover, it may integrate the logic ICs with microcontrollers or FPGAs (*Field Programmable Logic Arrays*) to handle real-time tasks or speed-critical operations.

Unfortunately, an open defect may occur at interconnects between gates inside the logic IC[4]. The defect may be caused by broken metal or polysilicon interconnects. It may cause incorrect logic behavior. Thus, it should be detected.

An ATE (*Automatic Test Equipment*) is one of a crucial role in detecting the defect[5]. It ensures that the IC functions correctly before shipping to markets. However, the ATE setup and programming require highly skilled and time-consuming.

The defect may be detected by a BIST (*Built-In Self-Test***)**[6].It is a DFT (*Design-for-Testability*) technique allowing the logic IC to test itself. It may improve test efficiency and reduce on external test equipment. However, it requires design complexity.

Other the proposed DFT is a scan chain testing[7]. It is a method designing flip-flops as a serial shift register during a test mode. Moreover, each of the flip-flops is to have a multiplexer at its input for selecting in normal mode. However, it takes design complexity.

Microscopy is proposed for detecting the defect[8]. It enables visual inspection and high-resolution imaging of the ICs at various scales from the macroscopic package level down to the atomic level. However, it is an expensive equipment.

The defect may be detected by a non-destructive technique of X-ray imaging[9]. It is used to visualize the internal structures without physically opening or damaging the IC. However, it requires specialized equipment and skilled in its operation.

An AC analysis was proposed to detect the defect[10]. The AC test signal is provided to inputs of the IC and response signals at its outputs are measured. However, the measured signals are amplitude and phase shift of specific frequencies in still steady state responses.

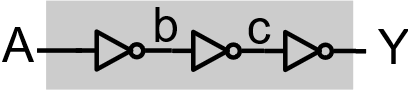
Full dynamic responses - both transient and steady-state – may be generated by a Laplace transform. The transform may analyze signals in complete performance view and sufficient stability analysis. Thus, the transform may be carried out to detect the defect.

In this paper, a Laplace transform is proposed to detect an open defect inside a logic IC. The IC is designed in a SPICE (Simulation Program with Integrated Circuit Emphasis) netlist library by Nexperia Co. Ltd[11]. Moreover, it is simulated using LTspice XVII produced by Analog Devices Inc[12]. The LTspice has available menu to implement the Laplace transform syntax.

# METHODS

A logic IC is used logic gates, combinational logic gates, and sequential logic gates implemented in digital logic functions. The gates are fundamental building blocks, i.e., AND, OR, NOT/ Inverter, NAND, NOR, XOR, XNOR, Multiplexers, Demultiplexers, Encoders / Decoders, Adders / Subtractors, Flip-flops, Counters, Shift Registers.

One of fundamental gates is an inverter. A logic diagram of the inverter is shown in **FIGURE 1**. It has an input A and an output Y. An open defect may occur at interconnects between gates inside the logic diagram, i.e., b and c nodes. The defect may be modeled in a resistance value. Larging the defect will increase the resistance value.



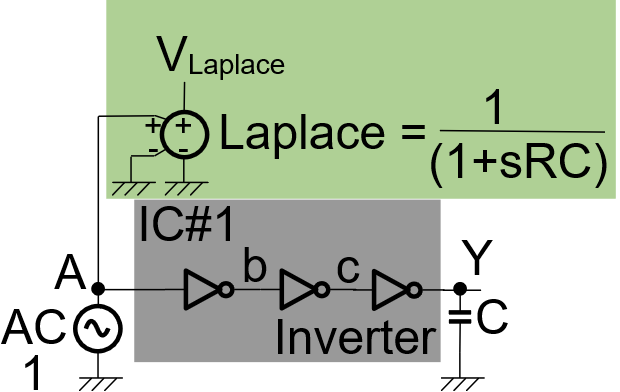
**FIGURE 1**. Logic Diagram of Inverter

Since the output Y is connected to load capacitance C, a transfer function of the inverter may be modeled by Equation 1. The function is used by a Laplace transform in algebraic equations (s-domain). Response signals of the output Y will match with responses of the Laplace transform.

(1)

# RESULTS AND DISCUSSION

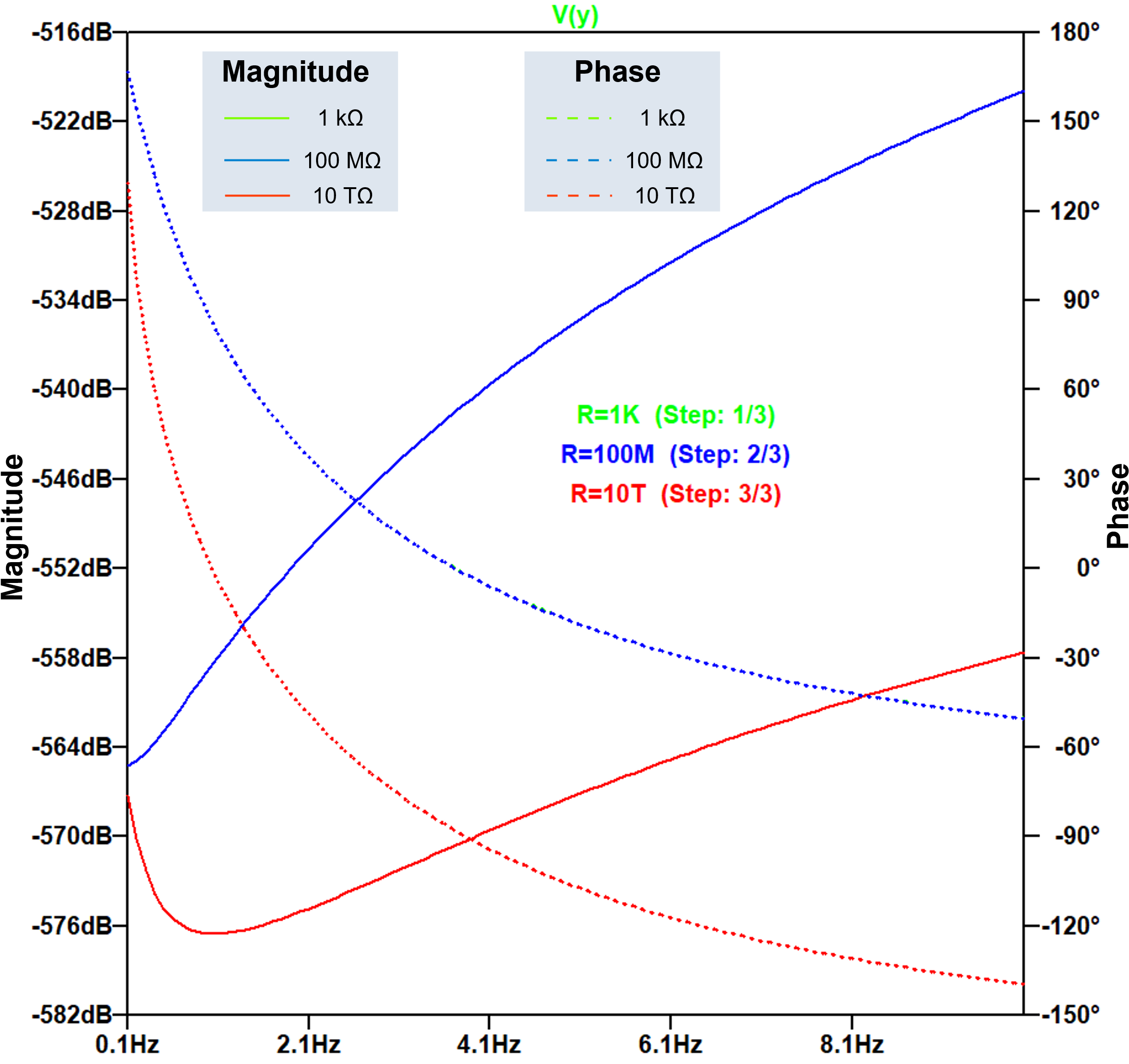
A Laplace transform is proposed to detect an open defect at an interconnect inside an inverter IC. The IC is shown in **FIGURE 2**. It is designed by a SPICE netlist library of Nexperia Co. Ltd. Moreover, a free SPICE simulator of LTspiceXVII produced by Analog Devices Inc is simulated it.



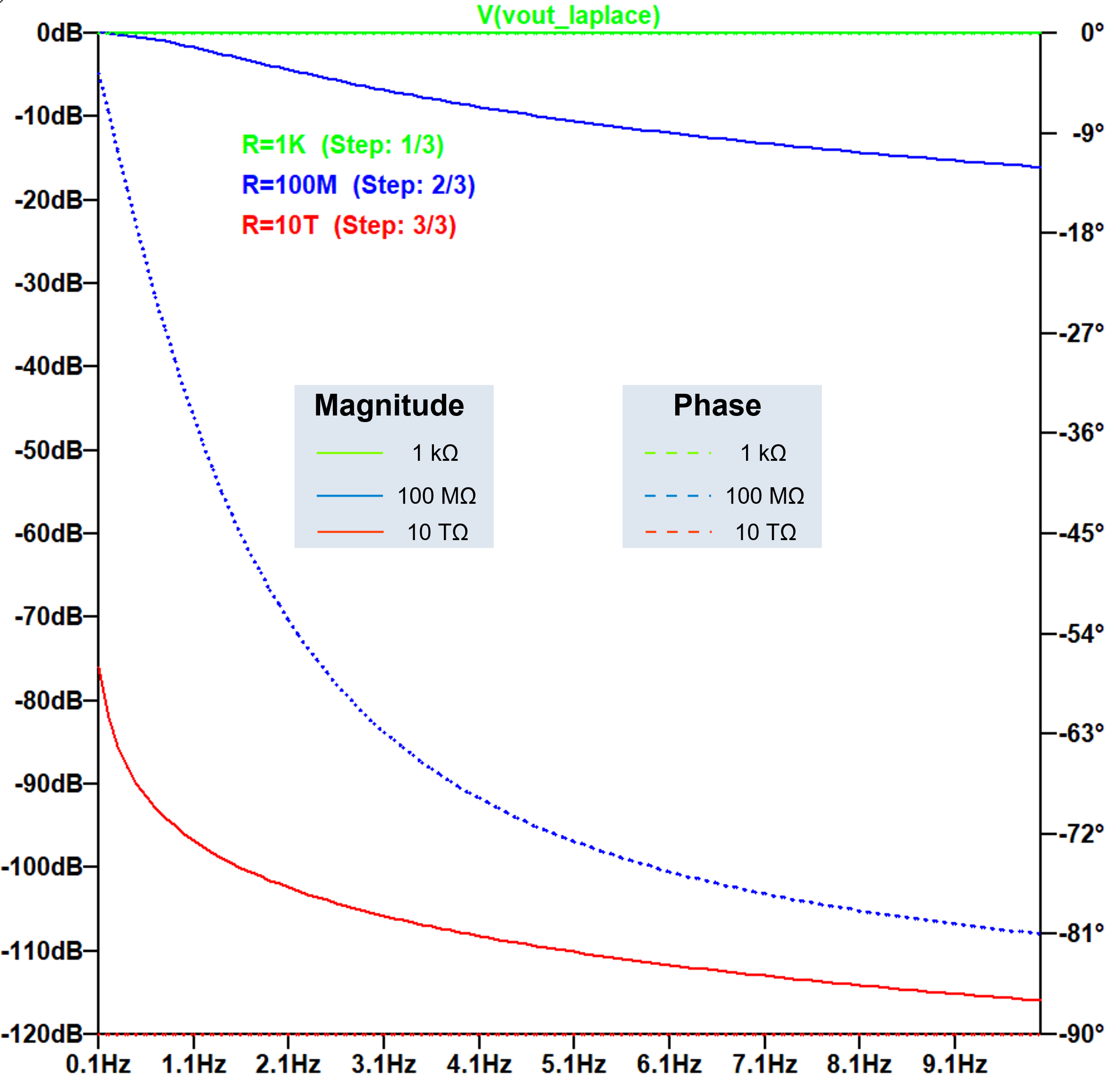
**FIGURE 2**. Inverter IC

The Laplace transform is modeled by Equation 1 in which it is implemented by a voltage dependent voltage source in the LTspiceXVII. The interconnect of *b* node inside the inverter IC is a targeted open defect. Resistors of 1 kΩ, 100 MΩ, 10 TΩ are inserted to the *b* node and to *R* in the Equation 1. Capacitor of 1 nF is provided to *C* in the Equation 1. An AC voltage signal of an amplitude 1 V is provided to the *A* input pin. Also, an AC analysis of linear type is provided by frequencies 0.1 Hz – 10 Hz.

A response signal generated by an output *Y* will match with a response of the Laplace transform, *VLaplace*. The output *Y* signal is shown in **FIGURE 3**.As shown in Figure 3, magnitudes of the *Y* signal increase linearly with increasing the defect. However, phases of the *Y* signal decrease linearly with increasing the defect. On the other hand, **FIGURE 4** showsthe *VLaplace* signal.Bothmagnitudes and phases of the *VLaplace* decrease linearly with increasing the defect.



**FIGURE 3**. Response signal of output *Y*



**FIGURE 3**. Response signal of output *VLaplace*

# CONCLUSIONS

A Laplace transform is proposed to detect an open defect inside an inverter logic IC. Resistors of 1 kΩ, 100 MΩ, 1 GΩ are inserted to the targeted open defect. A capacitor 1 nF is inserted to a load capacitance. The inverter IC is designed by SPICE netlist library and simulated by LTspiceXVII. Bothmagnitudes and phases of the *VLaplace* decrease linearly with increasing the defect.

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