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High-Performance Operational Amplifier Design Based on Current Recycling Technology

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High-Performance Operational Amplifier Design Based on Current Recycling Technology

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Abstract. This paper presents a current-recycled two-stage operational amplifier designed in 180nm CMOS optimized for applications requiring high gain and low power. This design based on current recycling technology employs trans-conductance boosting current mirrors ($K=3$), achieving a 105 dB open loop gain at a 108 μ W power consuming. RC compensation is designed to stabilized the amplifier, delivering a 7.7 Mhz unity-gain bandwidth while maintaining 60° phase margin. Measured performance shows a exceptional immunity to environmental interference, with 125 dB common-mode rejection ratio (CMRR) and 72 dB power supply rejection ratio (PSRR), enabling reliable operation in interference-prone environments. With 1.69 V output swing, the amplifier suits biomedical interfaces and IoT sensors. Future enhancements will focus on expanding bandwidth beyond 15 MHz through adaptive bias current tuning while maintaining sub-100 μ W operation. Additionally, migration to an advanced technology is proposed to improve temperature stability (-40°C to 125°C) and scalability down the supply power.

INTRODUCTION

Nowadays, operational amplifiers (op-amps) have become ubiquitous in modern electronic systems, as fundamental building blocks across diverse applications ranging from communication systems (e.g., radar and sonar signal conditioning) to biomedical instrumentation (e.g., neural signal acquisition) [1-2]. Operational amplifiers (op-amps) play a critical role in a wide range of applications, including signal processing, analog-to-digital converters (ADCs), digital-to-analog converters (DACS), and power management systems. Consequently, the design of a high-performance and energy-efficient op-amp holds significant importance in advancing modern electronic systems.

According to the requirements of high efficiency amplifier, the development of op-amps must achieve three conflicting objectives: 1) high voltage gain, 2) low power consumption for extended operational lifetime, and 3) compact silicon area for cost-sensitive applications. Therefore, finding a technology which can increase the gain and reduce the power consumption is critical.

In addition, the current recovery technology is based on the traditional cascode amplifier. Using the cascode amplifier did not provide gain with high transduction transistor, in the case of current and power consumption does not increase to achieve the purpose of improving the gain it has many advantages, is a good way to achieve low power consumption and high gain [3-4]. This study presents a novel amplifier architecture with high-gain and low-power consumption characteristics based on current-recycling technology [5]. The paper systematically elaborates on the innovative circuit design principles, encompassing theoretical derivations and numerical calculations from multiple dimensions including device parameter optimization, stability analysis, and frequency response characteristic modeling.

Following the introduction in Section 1, Section 2 elaborates on the circuit design methodology with 180nm CMOS technology, the design of the amplifier, bias circuits, and frequency compensation techniques. Section 3 presents the simulation framework, analyzes the experimental results, and evaluates the performance of the proposed

design. Finally, Section 4 concludes the study by summarizing the key findings, highlighting the contributions, and suggesting potential directions for future research.

CIRCUITS DESIGN

Measurement of Various Parameters for the 180-nm Technology

Because it is an unknown 180nm process, the characteristics of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) should first be measured by circuit simulation first to contribute to the circuits designing below with clearly analyzing the I/V characteristics of MOSFET [5].

To measure the characteristics of MOSFET, suitable simulation circuits are indispensable, and the IV curve needs to be analyzed after completing the circuit simulation, and λ (channel-length modulation coefficient), $k'(\mu_p C_{ox})$ and $\mu_n C_{ox}$ should be obtained [5]. Due to different properties, N-type MOSFET (NMOS) and P-type MOSFET (PMOS) should be simulated in different circuits as showed in Fig.1.

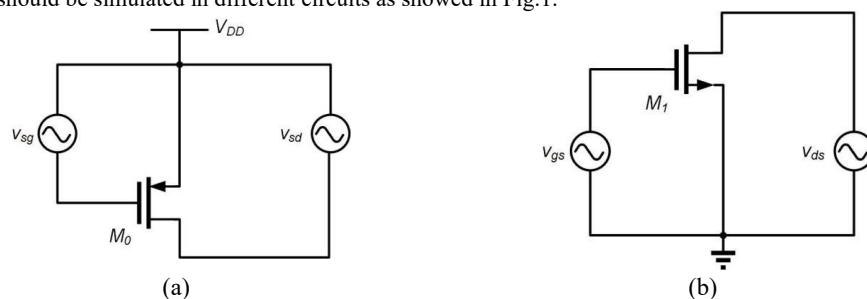


FIGURE 1. The simulation circuits of PMOS and NMOS, (a) is of PMOS and (b) is of NMOS.(Picture credit: Original)

From the EDA tools, the relationship between g_m (trans-conductance) and I_d (drain current of), between r_o (small-signal-equivalent resistance) and I_d of each transistor in all kinds of situations can easily be found with the simulation circuits.

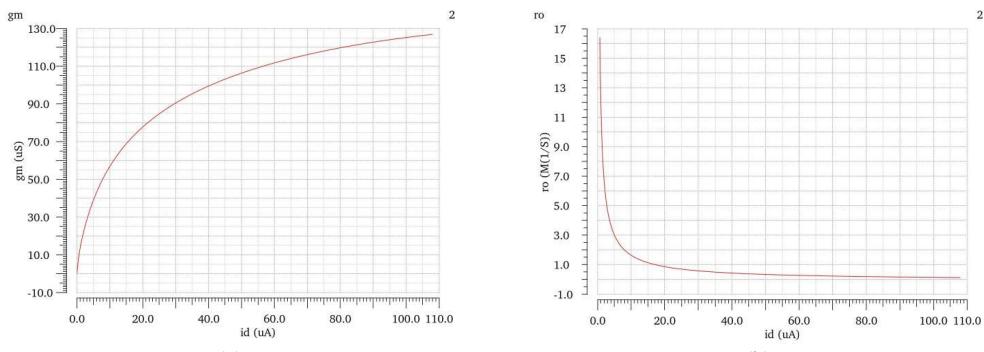


FIGURE 2. The result of PMOS simulation, (a) the relationship curves of g_m and I_d ; (b) the relationship curves of r_o and I_d .(Picture credit: Original)

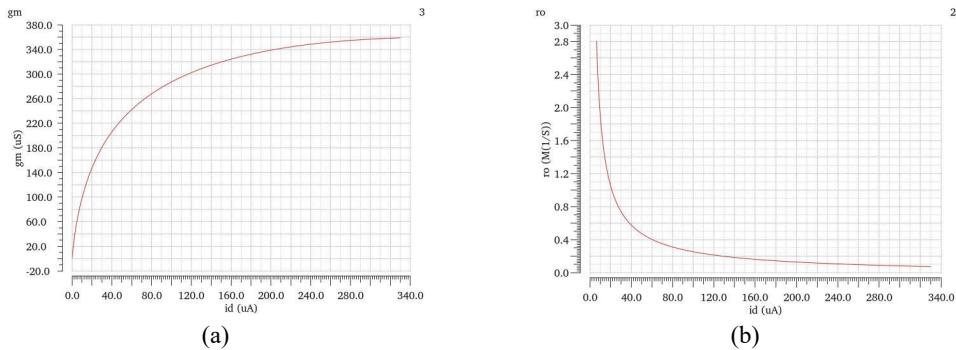


FIGURE 3. The result of NMOS simulation, (a) the Relationship curves of g_m and I_d ; (b) the Relationship curves of r_o and I_d .(Picture credit: Original)

Fig.2(a) and Fig.3(a) shows the relationship between g_m and I_d , and Fig.2 (b) and Fig.3 (b) shows the relationship between r_o and I_d , and results can be obtained according to the formula below [6]. (Both PMOS and NMOS are with the size of $W/L = 1\mu\text{m}/400\text{n}$)

$$r_o = \frac{I}{\lambda I_d} \quad (1)$$

$$g_m = \sqrt{2I_d \mu C_{ox} \frac{W}{L}} \quad (2)$$

Through the result from simulation EDA tools, the required parameters can be calculated. And the results are showed in Table.1.

TABLE 1. Parameters of needed transistors

TYPE	Channel Length Modulation Parameter: $\lambda(\text{V}^{-1})$	$\mu\text{Cox} (\text{uA/V}^2)$
PMOS	0.067	36.9
NMOS	0.042	114.4

Main Amplifier Design

The two-stage operational amplifier architecture has been established as the prevalent choice for high-gain implementations [7]. In this structure, the primary stage must be designed to maximize DC gain while maintaining low power consumption, whereas the secondary stage requires sufficiently low output impedance to ensure wide voltage swing and enhanced drive capability. This hierarchical approach achieves an optimal balance between small-signal amplification and large-signal output performance.

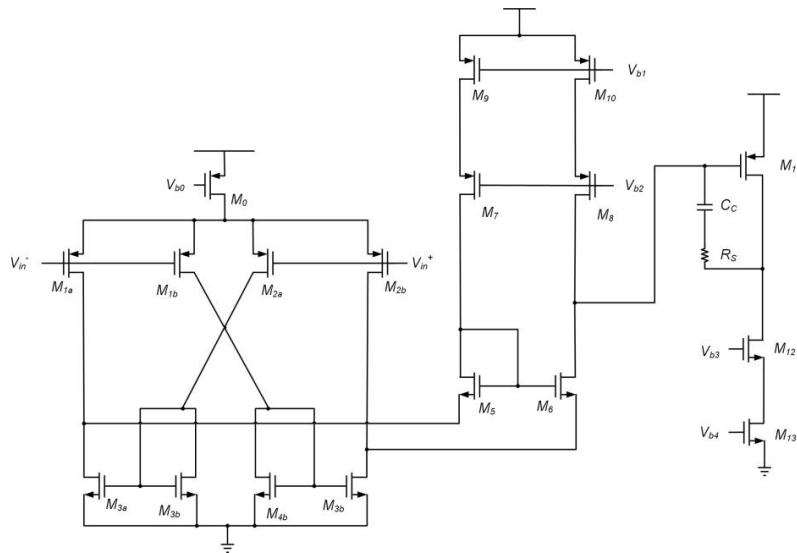


FIGURE 4. The main structure of the amplifier.(Picture credit: Original)

Firstly, as the structure showed in Fig.4, the first stage is designed with current recycling technology. For the first stage amplifier the trans-conductance not only comes from the gm transistors M1b and M2b, but also comes from M3b and M4b. Normally, the size of M3b and M4b is K times that of M1b and M2b, so the small signal current is K times that of M1b and M2b [8], the composite small-signal current becomes:

$$i_{out} = (I+K)g_{m1b}v_{id} \quad (3)$$

Therefore, the whole trans-conductor Gm is equal to (1+K) gm. Compared to the kind of traditional folded cascode, the current through M7-M10 is recycling to create trans-conductor and increasing the gain without additional current. This is why recycling technology can increase gain and decrease power consumption [9].

Subsequently, the role of the transistors M5 and M6 is Passive Current Mirror Load [10] to achieve the function of operational amplification. M5 can copy a small signal from right to left. Although this is not a strict current mirror, it can serve the same purpose.

The 2nd stage employs a common-source configuration to enhance drive capability. The output resistance of the 2nd stage amplifier is:

$$r_{out2} = r_{o11} \parallel g_{m12}r_{o12}r_{o13} \approx r_{o11} = \frac{I}{\lambda' I_{11}} = \frac{L}{\lambda' I_{11}} \quad (4)$$

To minimize output resistance, transistor M11 is designed with minimum channel length (180nm). At the same time, the current through transistor M11 should be large.

The gain of the 2nd stage:

$$A_{o2} = r_{out2}g_{m11} = \frac{L}{\lambda' I_{11}} \sqrt{\mu_p C_{OX} \frac{W}{L} I_{11}} = \frac{I}{\lambda'} \sqrt{\mu_p C_{OX} \frac{WL}{I_{11}}} \quad (5)$$

To increase the gain, with a relatively large current and minimum length, the width of M11 should be relatively large. The size of M11 is preliminary determined to be W/L=20um/180nm.

After the design of circuits, it is time to design the size of all transistors. Given the power of two amplifiers, the first stage is powered by 40 μ A, and the second stage is powered by 20 μ A, a relatively large current in the second stage is beneficial to driving ability and phase margin.

Back to the design of the first stage, to increase the gain, it is a good idea to use a relatively large channel length for its small λ , which means a bigger r_o . Considering decreasing the area the K should not be very big, and K = 3 is acceptable. The expression for the gain is derived as follows.

$$A_0 = G_m R_{out} \approx (I+K)g_{m1b}g_{m7}r_{op}^2 \times \frac{I}{2} \quad (6)$$

This formula is only an approximation of the gain, because the input operation point is not sure now and the size of two transistors is not sure. In this step, only finding the approximation is enough.

Cause it is just an approximation, the exact gain should come from simulation and the result is only for getting the size of transistors. To obtain a relatively high gain and considering the inaccurate estimation, size $W/L|_p=5\mu\text{m}/400\text{nm}$ is used. To ensure the N-type and P-type symmetry, $W/L|_n=2\mu\text{m}/400\text{nm}$. The size of M_5 and M_6 is up to the operation input voltage of the 2nd stage amplifier which is not sure and should be found from simulation.

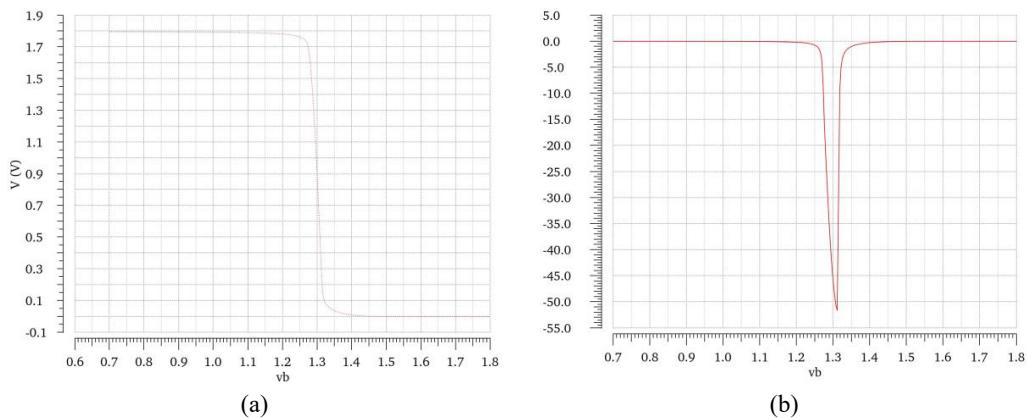


FIGURE 5. The result of 2nd amplifier DC simulation. (a) 2nd stage input output curve, (b) the derivative of (a). (Picture credit: Original)

According to Fig.5, the operation input voltage of the 2nd stage is 1.3112V . The output voltage of M_6 drain is,

$$V_{out1} = V_{ds3} + V_{gs5} = V_{ds3} + V_{TH6} + \sqrt{\frac{2I_6}{\mu_n C_{OX} \frac{W_6}{L}}} \quad (7)$$

With a constant length of transistor, systematic parametric analysis reveals an inverse correlation between M_5/M_6 transistor width and output voltage at the M_6 drain node. Using another simulation to scan voltages at different widths can obtain the size of M_5 and M_6 .

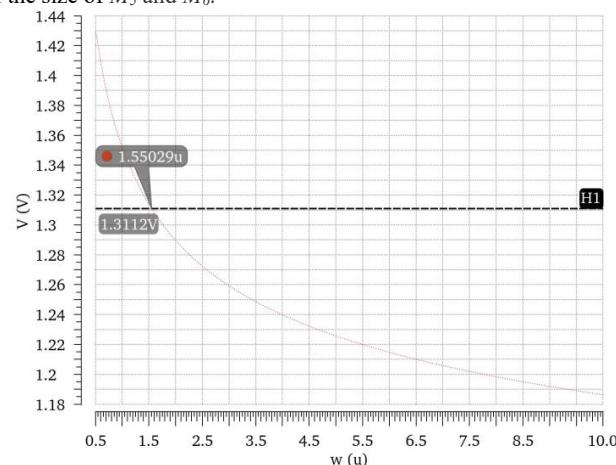


FIGURE 6. The input DC voltage of the 2nd stage amplifier with different widths of M_5 and M_6 . (Picture credit: Original)

According to Fig.6, it is clear that the width of transistors M_5 and M_6 should be $1.55\mu\text{m}$. So far, the sizes of all transistors have been determined.

Bias Circuits Design

The bias circuits are based on current mirror and channel length effect should be reduced [11].

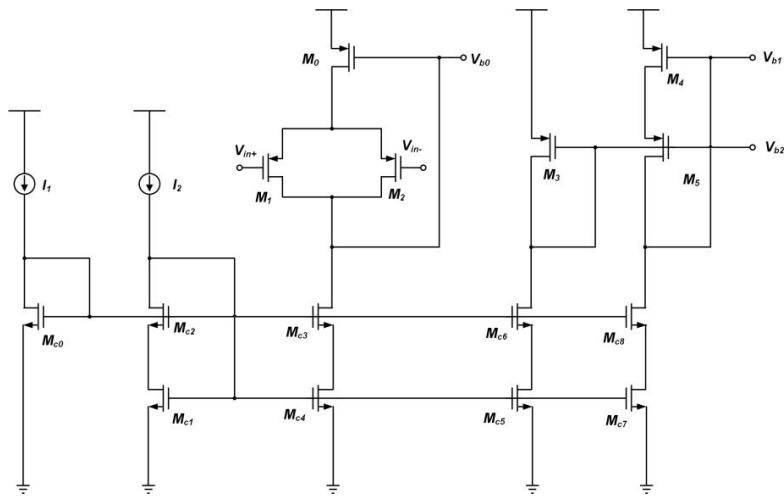


FIGURE 7. the structure of bias circuits.(Picture credit: Original)

As shown in Fig.7, M_{c0} to M_{c8} is a structure of low voltage cascode which can copy I_1 and I_2 , and M_3 to M_5 is the same low voltage cascode [12]. Low voltage cascode can reduce channel length effect and keep a low voltage of the transistor drain.

M_0 to M_2 is another way to reduce the channel length effect. The size of M_1 and M_2 should be twice that of M_{1a} to M_{2b} in Fig. 4, so the effect of input voltage to M_0 in Fig.8 and M_0 in Fig.4 will be the same. Therefore the drain and gate voltage of M_0 in Fig.8 and M_0 in Fig.4 will be the same, so the current of two will be matched well.

Frequency Compensation Techniques

To enhance the stability of the amplifier, the implementation of RC compensation is a good choice which serves as an established technique for inserting a left-half-plane (LHP) zero between the dominant pole and non-dominant pole [13]. A zero caused by RC compensation is a LHP zero which can cancel the effect of pole.

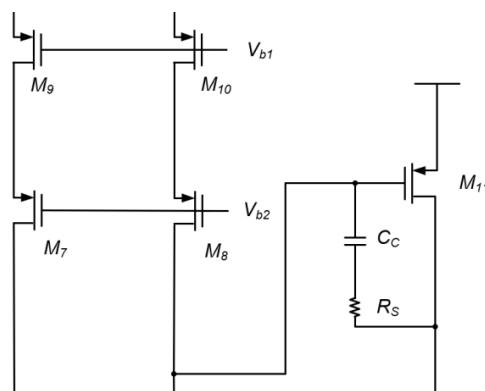


FIGURE 8. the structure of RC compensation(Picture credit: Original)

Fig. 8 shows the structure of compensation circuits, RS and CC create a feed-forward loop which causes a LHP zero. The formula of LHP zero as follows,

$$S_Z = \frac{I}{\frac{C_C}{g_{m11}} - R_Z C_C} \quad (8)$$

A suitable LHP zero can help a lot, and finally the value is $25\text{K}\Omega$ and 1.5pF (with a 50pF load)

SIMULATION ANALYSIS RESULT

Transient Analysis and AC Analysis

Both transient analysis and AC analysis are ways to find the output characters.

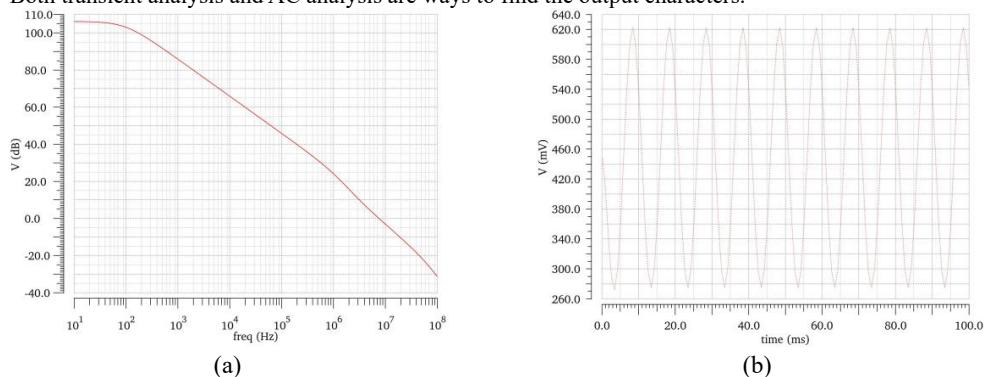


FIGURE 9. result of simulation a) AC analysis, b) Transient analysis with a $1\mu\text{V}$ input.(Picture credit: Original)

The amplifier demonstrates a low-frequency gain of 105 dB with 7.7 MHz unity-gain bandwidth, as evidenced in Fig. 9. This confirms a low-power operational amplifier structure achieving >100 dB gain-bandwidth efficiency.

Phase Margin and Output Voltage Swing

The phase margin can be found in AC analysis and phase analysis together.

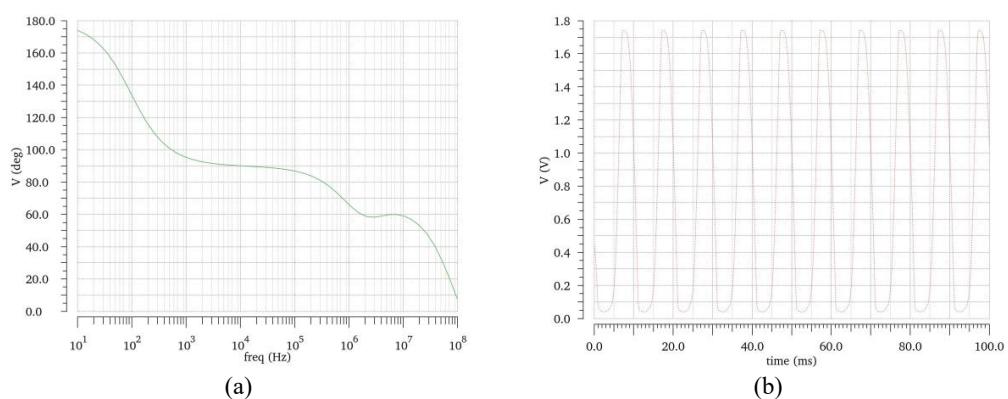


FIGURE 10. a) phase analysis, b) Transient output with a relatively large input.(Picture credit: Original)

As shown in Fig. 10 (a), the phase margin measures 60° at the unity-gain bandwidth (0 dB frequency). Fig. 10 (b) demonstrates an output voltage range of $1.74 V$ to $0.047 V$, while the DC operating point in Fig. 9(b) is centered at 456 mV. This configuration yields a total output swing of $818 mV$.

Common-mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR)

By applying a small-signal common-mode input, the CMRR can be evaluated through output response analysis; similarly, introducing a small-signal perturbation on the VDD supply permits determination of the PSRR from the output characteristics.

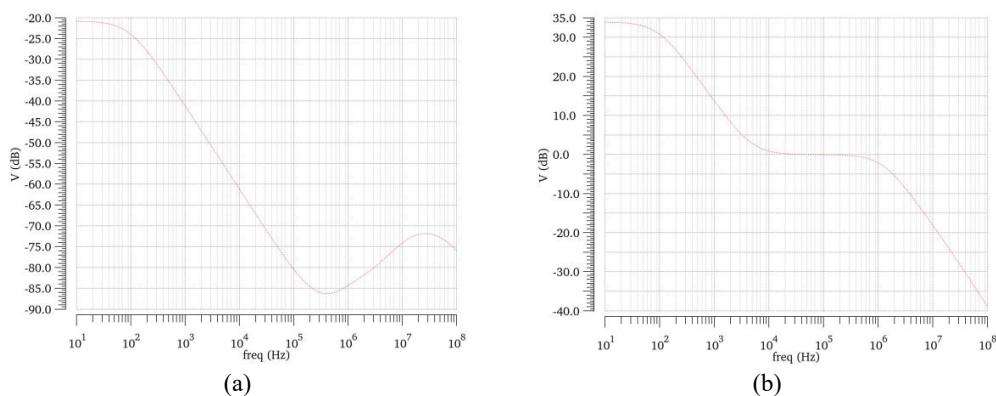


FIGURE 11. a) Common model input gain AC analysis, b) power source small signal gain AC analysis.(Picture credit: Original)

As demonstrated in Fig. 11 (a), the common-mode input gain measures -20.3 dB at low frequencies, yielding a CMRR of 125 dB. Correspondingly, Fig. 11 (b) shows a 33 dB small-signal source gain under similar conditions, resulting in a 72 dB PSRR.

Gain at different temperatures

At different temperatures, circuit performance may be affected. The temperature effects of this structure need to be further simulated.

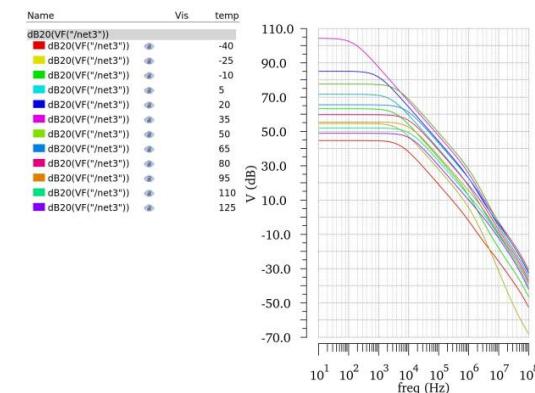


FIGURE 12. AC analysis at different temperatures.(Picture credit: Original)

From Fig.12 the highest gain appears at room temperature. No matter increasing or decreasing temperature, the gain will be lower.

CONCLUSION

This study proposes a two-stage operational amplifier architecture employing current recycling technology to achieve enhanced gain characteristics and power efficiency in 180nm CMOS process. Through innovative current mirror configuration ($K=3$ scaling factor), the design demonstrates 105dB DC gain with 108 μ W ultra-low power consumption, representing a 75% improvement in gain-power ratio compared to conventional folded cascode structures. The amplifier exhibits 7.7MHz unity-gain bandwidth and 60° phase margin when driving 50pF capacitive loads, ensuring stable operation in typical sensor interface applications. Particularly noteworthy are its exceptional common-mode rejection capabilities (125dB CMRR) and power supply noise immunity (72dB PSRR), critical for precision measurement systems.

The current recycling technology not only increases the gain by multiplying the trans-conductor by $1+K$ (in this study, $K=3$), but also decreases the power by reusing the current through M_{3a} and M_{3b} .

This amplifier offers diverse application scenarios across multiple industries. In the biomedical field, it serves as a critical component for physiological signal acquisition systems, including electrocardiogram (ECG) and electroencephalogram (EEG) sensor, implantable medical devices, and portable health monitoring solutions. For industrial applications, the amplifier demonstrates performance in processing signals from pressure sensors, strain gauges, as well as motion detection components like accelerometers and gyroscopes. Its precision characteristics make it suitable for scientific instrumentation applications such as spectrometer front-end signal conditioning and parameter acquisition modules in semiconductor testing equipment. The technology also finds important applications in energy and communication infrastructure, particularly in enhancing signal quality for radio frequency (RF) front-end circuits within base station architectures.

Future development directions will focus on performance enhancements through technological innovation. Engineering efforts will prioritize expanding operational bandwidth to support emerging ultra-high-speed circuit applications. Circuit optimization initiatives aim to improve power supply rejection characteristics, reducing system sensitivity to voltage source fluctuations. Advanced manufacturing processes will be explored to enhance thermal stability and enable operation at lower supply voltages, addressing performance degradation challenges associated with temperature variations.

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