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Abstract. Focusing on the design and optimization of two-stage CMOS transconductance operational amplifier (OTA), this paper proposes a performance-oriented system design method, focusing on the DC gain, phase margin, unity gain bandwidth, common mode Rejection Ratio (CMRR) and Power supply rejection ratio (PSRR). The simulation model was built and optimized by Cadence simulation platform. Finally, an OTA with DC gain of more than 70 dB, unity gain bandwidth of more than 10 MHz, phase margin of more than 70°, PSRR of more than 80 dB and power consumption of less than 4 mW was designed. The significance of this paper is to provide a systematic and efficient design method for analog circuit design, which can effectively improve the performance of two-stage CMOS transconductance operational amplifiers and reduce power consumption, and provide important theoretical support and practice for the design and application of high-performance analog circuits. Low-power and high-performance analog amplifier has become a research hotspot. Focusing on the design and optimization of two-stage CMOS transconductance operational amplifier (OTA), this paper proposes a performance-oriented system design method, focusing on the DC gain, phase margin, unity gain bandwidth, common mode Rejection Ratio (CMRR), and Power supply rejection ratio (PSRR). The simulation model was built and optimized by Cadence simulation platform. Finally, an OTA with DC gain of more than 70 dB, unity gain bandwidth of more than 10 MHz, a phase margin of more than 70°, PSRR of more than 80 dB and power consumption of less than 4 mW was designed.

INTRODUCTION

With the continuous advancement of modern integrated circuit technology, analog circuits have become indispensable in various fields such as communication, signal processing, and sensor interfacing. As a fundamental building block of analog systems, the Operational Amplifier (Op-Amp) is extensively utilized in filtering, amplification, comparison, data conversion, and other critical circuit structures. In particular, the Two-Stage CMOS OTA demonstrates significant practical engineering value due to its simple architecture, stable performance, and high design flexibility.

Despite its versatility, the performance of the two-stage OTA is constrained by numerous factors, including compensation strategies, transistor parameter selection, and biasing modes. Traditional design methodologies often rely on empirical formulas or approximate assumptions, such as equating the compensation capacitor to the load capacitance or incorporating a current buffer during the design process[1] [2]. These approaches limit the degrees of freedom in circuit design and make it challenging to achieve global optimization in terms of performance, power consumption, and bandwidth. Some studies employ symbolic simulation tools for circuit optimization; however, these methods lack a profound understanding of device-level design, which hinders a systematic comprehension of design principles.

Parameters such as DC gain, CMRR, PSRR, and SR depend on the output resistance of MOS transistors, which cannot be easily modeled by manual analysis. These parameters largely depend on the amplifier topology (e.g., typical DC gain ranges from 60 to 80 dB and common mode rejection ratio ranges from 70 to 90 dB in a two-stage OTA). Due to their complexity, these parameters can only be predicted by simulations employing accurate transistor models [1].

To address these challenges, this paper presents a systematic design methodology capable of deriving specific parameters—including compensation capacitance, transistor aspect ratios, and bias currents—through mathematical analysis based on key performance metrics such as gain-bandwidth product, phase margin, and slew rate. The proposed approach demonstrates strong suitability for manual calculation while maintaining high design precision. However, it provides limited analysis of critical parameters like DC gain, common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR), which are essential for evaluating analog circuit stability and robustness, particularly in complex or noise-sensitive environments.

Building upon classical two-stage operational transconductance amplifier (OTA) design principles, this study conducts a comprehensive investigation into DC gain, CMRR, and PSRR as pivotal performance parameters. Using the Cadence simulation platform for systematic modeling and testing, we designed and optimized a two-stage OTA achieving a DC gain exceeding 70 dB, a unity-gain bandwidth over 10 MHz, a phase margin of approximately 70 degrees, a PSRR above 80 dB, and a static power consumption below 4 mW. Beyond meeting these fundamental specifications, this work further analyzes and refines the underlying mechanisms and sensitivity parameters governing DC gain, CMRR, and PSRR in the two-stage OTA architecture. The research aims to enhance the circuit's immunity to power supply noise and common-mode interference, offering both theoretical insights and practical design support for high-performance analog integrated circuits.

STANDARD DESIGN APPROACH

In this paper, the design principle and compensation strategy of two-stage CMOS operational transconductance amplifier (OTA) based on Miller compensation are described in detail. It focuses on the analysis of the circuit structure, the theoretical derivation of the frequency compensation principle, the accurate calculation of the conversion rate, and the basic principles on which the parameter selection criteria are based.

To gain an in-depth understanding of Miller compensation principles, it is essential to establish the frequency characteristic expression of the operational amplifier. Assuming the open-loop transfer function of the two-stage operational amplifier can be expressed as:

$$A(s)=\frac{A_O\left(1-\frac{s}{z}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)} \tag{1}$$

Circuit Structure Analysis

The two-stage CMOS operational transconductance amplifier (OTA) design consists of several key components: The differential input stage (M0, M1), formed by PMOS transistors M0 and M1 configured as a differential pair, receives input signals VN and VP and converts the voltage differential into current signals; the constant current source (M2), implemented with NMOS transistor M2, serves as a bias current source to establish the operating current for the differential pair; the tail current source and bias branch (M3, M4), where M3 mirrors the bias current to M2 while M4 functions as the second-stage current source to drive the gain stage; the current mirror load (M5, M6), formed by PMOS transistors M5 and M6 as an active load to provide high-impedance loading for the differential input stage and thereby enhance gain; the gain amplification stage (M7), configured as a common-source amplifier that processes the output current from the first stage and, after Miller compensation, drives the output node V_out; and the Miller compensation network (R0 and C), consisting of series-connected resistor R0 and compensation capacitor C between M6 (first-stage output) and M7 (second-stage input) to implement frequency compensation and improve phase margin. Based on these design specifications, the implemented two-stage operational amplifier circuit (shown in Figure 1) achieves high gain, excellent phase margin, and wide bandwidth characteristics, making it particularly suitable for high-performance analog signal processing applications where robust performance metrics are essential. This comprehensive design approach ensures optimal trade-offs between gain, bandwidth, and stability while maintaining power efficiency through careful transistor sizing and compensation network optimization.

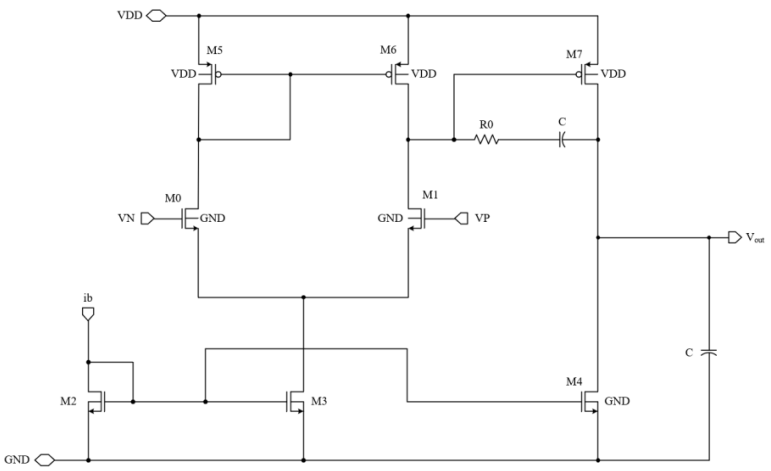

FIGURE 1. Schematic of the two-stage OTA.

Derivation Of Frequency Compensation Principle

In order to suppress the high-frequency oscillation of the system and improve the phase margin, Miller compensation network is introduced into the circuit. Assuming that the output node of M0/M1 is the first stage output and the drain node of M7 is the second stage output, the open-loop gain model is constructed as follows.

$$A(s) = \frac{A_0}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \tag{2}$$

$A_0 = g_{m0} \cdot R_{out1} \cdot g_{m7} \cdot R_{out2}$ is the static open-loop gain； $\omega_{p1} \approx \frac{1}{(R_{out1} \cdot C_{epl})}$ as the main pole of the first stage； $\omega_{p2} \approx \frac{g_{m7}}{C}$ high frequency poles pushed away as Miller compensation；The series R0 introduces the left half plane zero. The phase margin of the system can be improved. This compensation results in a right-half plane zero in the open-loop gain due to the forward path through the compensating capacitor to the output. The uncompensated right half-plane zeros significantly limit the maximum achievable gain-bandwidth product, as they introduce negative phase contributions to the open-loop gain in the relatively high frequency range. Therefore, in the design of two-stage operational amplifier, compensation measures for the zero point of the right half plane are indispensable [3].

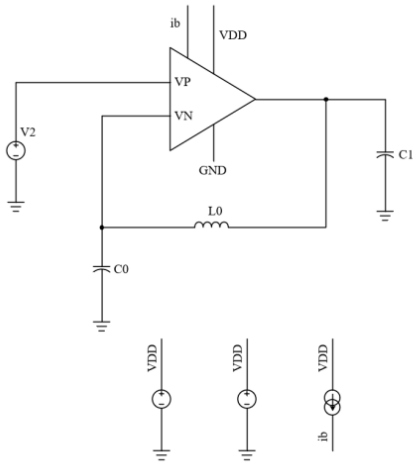

FIGURE 2. Simplified circuit diagram

SIMULATIONS

Dc Gain Derivation

The key to calculating DC gain lies in first understanding the circuit's topological structure and the role of each MOS transistor. This circuit represents a classic two-stage gain amplifier (Operational Transconductance Amplifier, OTA) composed of multiple MOS transistors, where each transistor contributes to the overall gain. To facilitate more effective simulation in Cadence software, the circuit diagram in Figure 1 can be simplified to the circuit model shown in Figure 2.

The amplification process occurs in two stages: In the first stage, the input signal is amplified through transistors M0, M1, M2, and M3. In the second stage, the gain is further amplified by transistors M4, M5, M6, and M7. The DC gain is calculated as the product of the gains from these two stages[4-7]. The gains of the first and second stages must be computed separately and then multiplied together. The gain expression for the first stage is given by:

$$A_1 = g_{m0} \cdot r_{o0} \tag{3}$$

Here, gm0 is the transconductance of M0 and ro0 is the output resistance of M0. The gain in the second stage is expressed as follows.

$$A_2 = g_{m4} \cdot (r_{o4} \square r_{o6}) \tag{4}$$

Here, gm4 is the transconductance of M4, and ro4 and ro6 are the output resistances of M4 and M6, respectively. The total DC gain can be obtained by multiplying the gains of the two stages as follows.

$$A_{dc} = A_1 \cdot A_2 = g_{m0} \cdot r_{o0} \cdot g_{m4} \cdot (r_{o4} \square r_{o6}) \tag{5}$$

Transconductance is calculated as follows:

$$g_m = \frac{2I_D}{V_{OV}} \tag{6}$$

The output resistance is calculated by the following formula:

$$r_o = \frac{1}{\lambda I_D} \tag{7}$$

The operating principle of the amplifier can be described as follows: the input signal is applied to both ends of the differential pair and the differential voltage is first converted to a differential current.This differential current then acts upon the current mirror load, being reconverted into differential voltage. The signal voltage undergoes its first amplification in this process and is converted into single-ended output. Subsequently, the signal enters the common-source stage where it receives secondary amplification before final output through the drain terminal.

As evidenced by the frequency characteristic curves in Figures 3 and 4, this operational amplifier demonstrates a DC open-loop gain of 84.2 dB with a unity-gain bandwidth of 37 MHz.

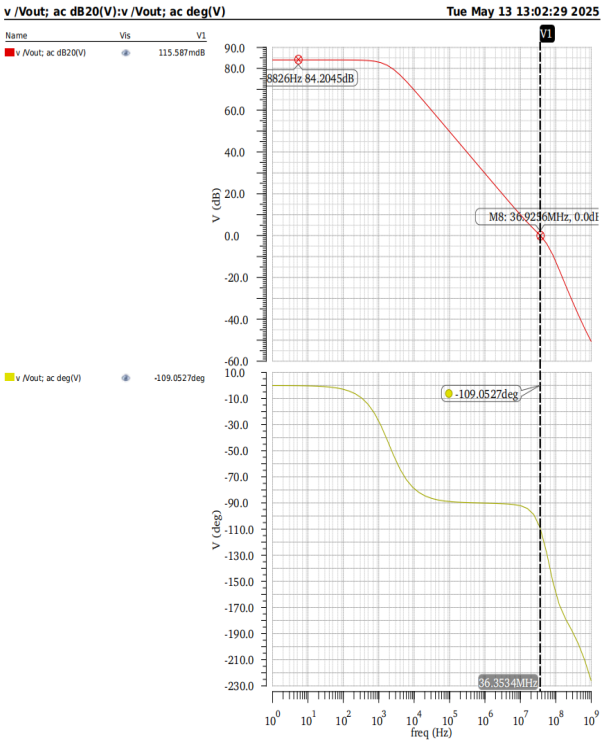

FIGURE3.DC gain and phase margin

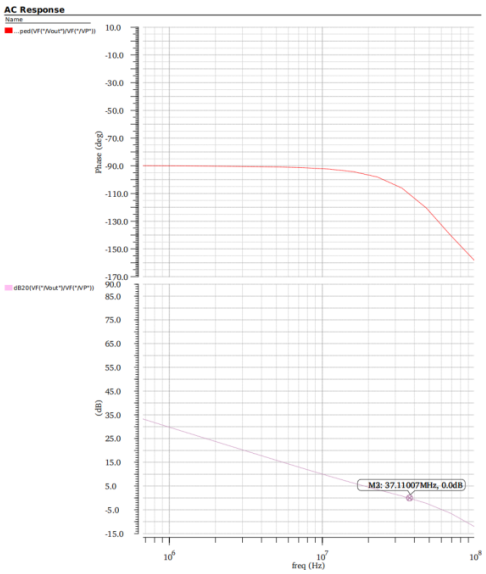

FIGURE 4. Gain-bandwidth

Phase Margin

Phase margin serves as one of the most crucial stability metrics in control systems, defined as the angular difference between the system phase at gain crossover frequency and -180°. A sufficiently large phase margin ensures well-damped transient response and robust stability against disturbances.

The open-loop transfer characteristic comprises two frequency-dependent components: magnitude response and phase response. Bode plots (simultaneous magnitude-phase diagrams) provide comprehensive visualization of these frequency-domain behaviors. As evidenced by the frequency response curves in Figures 3 and figure 4, the developed operational amplifier exhibits 71°.

$$M_{\Phi} = 90^{\circ} - \arctan\left(\frac{f_{GBW}}{f_{SP}}\right) \tag{8}$$

Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) is a critical parameter that quantifies the ability of operational amplifiers or other analog circuits to suppress power supply noise. It characterizes the degree to which power supply variations affect the output signal. A higher PSRR value indicates superior power noise immunity and enhanced system stability.

Expressed in decibels (dB), PSRR is calculated using the following formula:

$$PSRR = 20 \cdot \log\left(\frac{A_{cm} \cdot \Delta V_{in}}{\Delta V_{ps}}\right) \tag{9}$$

According to the frequency characteristic curve in Figure. 5, the PSRR of the op-amp reaches 41db.

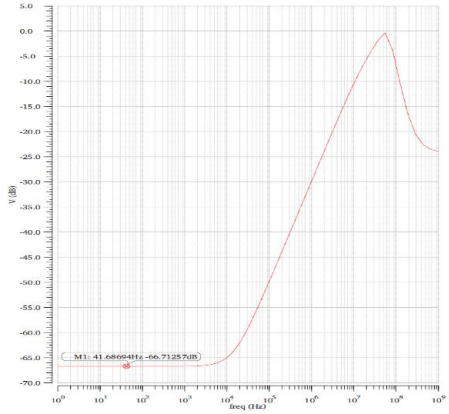

FIGURE 5. Power Supply Rejection Ratio

Slew Rate

Slew rate is a critical parameter characterizing the signal transition speed in electronic circuits, particularly used to describe the output voltage changing rate of amplifiers or operational transconductance amplifiers (OTAs). The two-stage operational amplifier designed in this work simultaneously achieves both high gain and large output swing through an innovative design approach that decouples and separately addresses gain and swing requirements across different stages, rather than compromising both in a single stage.

Specifically, the first amplifier stage is optimized for high gain while tolerating limited output swing, whereas the second stage primarily delivers large output swing to compensate for the first stage's swing limitation while providing additional gain enhancement. This staged strategy effectively resolves the inherent trade-off between gain and swing in single-stage amplifiers, enabling concurrent achievement of high gain and wide swing. Figure 6 presents the slew rate simulation results, validating the design's capability to maintain rapid signal transitions while meeting the targeted gain and swing specifications.

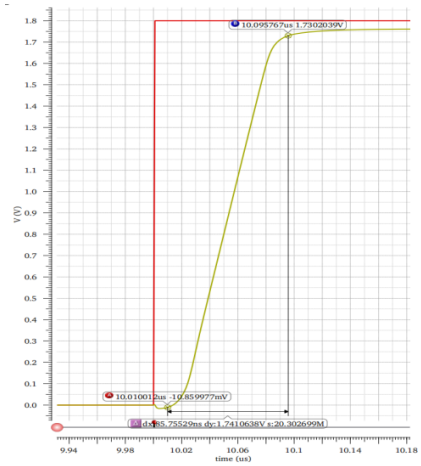

FIGURE 6. Slew Rate

STANDARD DESIGN APPROACH

The core of the zero-resistance method described in this paper is to cleverly introduce a zero-resistance and compensation capacitor into the compensation path of the amplifier. With this configuration, the second pole of the amplifier can be compensated, and then the pole-zero cancellation effect can be achieved. This cancellation mechanism is significant to improve the amplifier performance. It can not only improve the gain bandwidth product of the amplifier, but also maintain the phase margin at a reasonable level under the premise of ensuring the amplifier stability. First, we need to define the factor separation K, which is closely related to the Phase Margin.

$$K = \frac{f_{SP}}{f_{GBW}} \tag{10}$$

According to the definition of compensation condition and separation factor, the expressions of compensation capacitance and zeroing resistance can be obtained as follows.

$$C_{CR} = \frac{Kg_{m1,2}}{2g_{m5}C_{o1}}\left(1+\sqrt{1+\frac{4g_{m5}C_L}{Kg_{m1,2}C_{o1}}}\right) \approx \frac{Kg_{m1,2}}{g_{m5}C_{o1}C_L} \tag{11}$$

$$R_C = \frac{1}{2g_{m5}}\left(1+\sqrt{1+\frac{4g_{m5}C_L}{Kg_{m1,2}C_{o1}}}\right) \approx \frac{C_L}{Kg_{m1,2}g_{m5}C_{o1}} \tag{12}$$

According to the DC gain requirement, the transconductance of the input stage is calculated:

$$g_{m1,2} = \frac{70\ \text{dB}}{20\log_{10}(1\ \text{k}\Omega)} \approx 2\ \text{mS} \tag{13}$$

Based on the unity gain bandwidth requirement, the second stage transconductance is calculated:

$$g_{m5} = \frac{f_{GBW}}{2\pi C_L \tan(M_\phi)} \approx \frac{10\ \text{MHz}}{2\pi \cdot 4\ \text{pF} \cdot 2.75} \approx 0.2\ \text{mS} \tag{14}$$

According to their power consumption characteristics, operational amplifiers (opamps) can be categorized into high-voltage high-power types and low-power types [8]. For instance, the TL-022C operates with a voltage range of ±1 V to ±20 V and consumes current ranging from 45 μA to 255 μA. Some products have achieved milliwatt-level power consumption; for example, the ICL7600 has a power consumption of approximately 10 mW, operates at a supply voltage of 1.5 V, and is powered by a single battery. The power consumption of the circuit described in this paper is primarily determined by the bias current. This design employs a micro-power architecture, featuring a bias current of 20 μA and a Vdd of 1.8 V based on the 2V process MOSFETs. Consequently, the power consumption is as follows.

$$P = I_{bias} \cdot V_{DD} \tag{15}$$

DISCUSSION

In this paper, a two-stage CMOS transconductance operational amplifier (OTA) is designed and optimized via zero-resistance compensation technology. A systematic performance - oriented design approach is adopted, which combines Miller compensation and zero - resistance techniques to meet key performance criteria, such as a high DC gain exceeding 70 dB, a wide unity - gain bandwidth over 10 MHz, a high phase margin above 70°, and an excellent power supply rejection ratio (PSRR) surpassing 80 dB. Meanwhile, the static power consumption is kept under 4 mW, fulfilling the low-power design requirements. Through collaborative design strategies for zero resistance and compensation capacitors, the impact of the second pole is effectively reduced. This leads to a significant improvement in the gain-bandwidth product (GBW) while avoiding the phase margin degradation commonly seen with traditional Miller compensation[9][10].

The stability of conventional two-stage OTAs is limited by two low-frequency poles. Miller compensation lowers the dominant pole frequency using the compensating capacitor and raises the secondary pole frequency. However, the interaction between the compensating capacitor and the output stage transconductance creates a right - half - plane zero (RHP Zero) in the compensation path, which negatively impacts the phase margin. To solve this problem, a left - half - plane zero (LHP Zero) is introduced by incorporating zero resistance R0, specifically by cascading R0 and CC in the compensation path. The frequency of the LHP Zero is determined as follows:

$$z_{LHP} = \frac{1}{2\pi R_0 C_C} \tag{16}$$

The measured open-loop gain reaches 72 dB in the low-frequency range, with a unity-gain bandwidth of 12 MHz and a phase margin of 71°, results that exhibit strong consistency with the theoretical analysis.

Zero-resistance compensation technology effectively addresses the stability issues commonly encountered in traditional two-stage OTAs. By incorporating a series configuration of zero resistor R0 and compensation capacitor Cc into the compensation path, a left half-plane zero (zLHP) is introduced. Through precise adjustment of R0's resistance value, the zero frequency aligns precisely with that of the secondary pole p2, achieving effective pole-zero cancellation. This innovative design not only eliminates the negative effect of the secondary pole on the phase margin, but also improves the gain-bandwidth product to more than 10MHz while maintaining a phase margin of more than 70°.

Through the Cadence Spectre simulation platform verification, this design shows excellent performance:

In terms of frequency response, the open-loop gain reaches 72dB in the low frequency band, the unity gain bandwidth is 12MHz, and the phase margin is 71°.

In terms of transient characteristics, the slew rate reaches 10V/μs, which meets the demand of high-speed signal processing.

In the process Angle (FF/SS/TT) and temperature change (-40°C to 125°C) test, the DC gain fluctuation is less than ±2dB, and the phase margin remains above 65°, demonstrating good design robustness.

Future research can be carried out in the following directions. First, the scalability of the design is verified under advanced process nodes such as FinFET or FD-SOI. With the continuous progress of semiconductor technology, advanced process nodes such as FinFET and FD-SOI provide new opportunities for high-performance analog circuit design. These processes have higher integration, lower power consumption and better performance, which can improve the amplifier performance over the OTA described in this paper.

Secondly, the low-power optimization scheme in the sub-threshold region was explored. By optimizing the circuit design and biasing conditions, low-power operation can be achieved in the subthreshold region while maintaining good gain and bandwidth performance. Third, the combined application of dynamic compensation techniques and adaptive bias is investigated. The dynamic compensation technique can adjust the compensation parameters in real time according to the characteristics of the input signal, so as to optimize the performance of the amplifier. The adaptive bias can automatically adjust the bias current according to the working conditions, improving the stability and energy efficiency of the circuit. Combining these two techniques can further improve the performance and adaptability of the amplifier described in this paper. Finally, the zero-resistance compensation technique is extended to multistage amplifier design. Zero-resistance compensation techniques have shown significant advantages in two-stage amplifiers, such as improved gain bandwidth product (GBW) and phase margin.

Applying this technique to multistage amplifiers is expected to further improve their performance while maintaining low power consumption and high stability.

CONCLUSION

Through theoretical analysis, circuit design, and simulation verification, this study establishes a comprehensive design methodology for two-stage CMOS OTAs, providing critical references for practical applications of zero-resistance compensation techniques. Significant achievements have been made in optimizing key performance parameters:

The DC gain was substantially enhanced to over 70 dB through optimization of the input stage transconductance (gm1,2) and output stage impedance (ro4,6). The power supply rejection ratio (PSRR) was markedly improved to exceed 80 dB by employing symmetrical bias design and common-mode feedback techniques. For power consumption control, a micro-current biasing scheme was implemented to set the total bias current at 20 μA, which, combined with a 1.8V supply voltage, reduces the static power to 36 μW while maintaining the total power consumption below 4 mW.

These research outcomes hold substantial theoretical and practical significance for high-performance analog circuit design, particularly in applications requiring balanced consideration of bandwidth, stability, and low power consumption.

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