Optimization Study Based on Folded Common-source, Common-gate Op-amps

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Abstract. In the field of modern high-precision analog signal processing, folded cascode op amps are a key component in the circuit module because of their combination of high gain and wide swing. With the continuous improvement of the performance requirements for operational amplifiers in applications such as high-speed and high-precision data converters and sensor interfaces, optimizing the mismatch characteristics of folded common-source and common-gate operational amplifiers has become an important research direction in the design of analog integrated circuits. However, the mismatch of its devices is a non-negligible constraint on the performance improvement. In this paper, the voltage gain of this op-amp is derived based on a small signal model. Optimization of circuit structure for folded cascode op amps and analysis of advantages and disadvantages. And mismatch analysis is performed based on the folded cascode op amps structure. By analyzing the structural design and circuit design ideas of folded cascode op amps, the possible mismatches and misadjustments in the circuits are analyzed to provide a theoretical basis for the design and planning of high-performance op-amps.

INTRODUCTION

As one of the analog integrated circuit modules, folded common source and common gate amplifiers have more obvious advantages in terms of high gain, high bandwidth and anti-noise performance, and are widely used in high-speed communication, sensor interface and precision data conversion. The structure effectively improves output impedance and gain by stacking common source and common gate (Cascode) stages, while the differential architecture enhances system robustness by suppressing common mode interference.

In recent years, with the high-speed development of 5G/6G communication, Internet of Things, and intelligent sensing technology, there is a high demand for signal processing and amplification in different fields, throughout the wireless communication, industrial sensing, aerospace, medical equipment, and other modern technology fields. The problems of performance and reliability of conventional amplifier structures are increasing, so the problems of enhancing the performance of circuit structures and reducing circuit mismatches need to be solved. Currently, in 5G and millimeter communications, a unit gain bandwidth of 20 GHz and a phase margin of 68 degrees have been achieved by introducing distributed interstage compensation capacitors and optimized cascade current mirrors. It is suitable for high-speed SerDes interface circuits [1]. Low power requirements for Internet of Things (loT) devices [2]. By adjusting the bias of the tail current in real time, the static power consumption is reduced by 50% while still maintaining 85dB of gain and 10 MHz of bandwidth per unit gain. It incorporates a “segment bias” control logic that switches the operating mode according to the dynamic range of the input signal, significantly improving the energy efficiency ratio.

Therefore, in this paper, the structures of folded common-source common-gate op-amps as well as sleeve common-source common-gate op-amps are compared. The gain of the folded common-source common-gate op-amp is derived and the structure of the folded op-amp is optimized. The mismatch that occurs in the optimized folded op-amp is analyzed, as well as the structural advantages and disadvantages of the folded op-amp in terms of performance.

PRINCIPLE OF FOLDED COMMON-SOURCE, COMMON-GATE AMPLIFIER TO INCREASE GAIN

Folded Common Source and Common Gate Level Op-Amp Study

Mir Bintul Islam et al. modeled a high-gain, low-power folded common-source, common-gate operational transconductance amplifier (FC-OTA) by using the HSPICE software [3]. Among the FC-OTA designs are CNFETs, GNRFETs, and hybrid implementations combining CNFETs and CMOS.

Among the FC-OTA designs are CNFETs, GNRFETs, and hybrid implementations combining CNFETs and CMOS. Significant improvements in DC amplification, output resistance, average power dissipation, and common-mode rejection ratio are achieved compared to conventional CMOS-based FC-OTA. In addition, Israa Mohammed et al. were able to substantially improve the performance of folded common-source, common-gate CMOS operational transconductance amplifiers (OTAs) by means of a water-cycling algorithm (WCA)[4]. Since WCA has an efficient global search as well as local search capability, the voltage gain is significantly increased and the gain bandwidth is substantially increased compared to the no-algorithm. This design solution provides significant high-frequency amplification and the lowest power consumption. Naushad Manzoor Laskar et al. proposed a new approach to high-performance analog amplifier circuits- Ring Fold Common Source Common Gate (RFC) amplifiers [5]. The amplifier is an enhanced version of the conventional folded common source and common gate amplifier. Acting on the same area as well as power budget, it has better performance in terms of gain, bandwidth, conversion rate, and misalignment. In addition, swarm optimization techniques have been applied in determining the optimal size of RFC amplifiers, allowing area minimization while satisfying other constraints.

Advantages of Folded Common Source Common Gate Op Amps

The common-source, common-gate structure has the advantage of high input and output impedance as well as high gain. The idea behind the design of this circuit is to convert the input voltage of the circuit into a current and then use the current as the input to the common gate. The structural disadvantages of the sleeve-type common-source, common-gate operational amplifiers are the small output swing and the difficulty of creating a short-circuit condition between the input and output. However, folded common-source, common-gate operational amplifiers are characterized by more than just the high speed and large bandwidth of the sleeve structure op-amps. And the folded type also features a larger output swing and a larger common-mode input range. In addition, the folded common-source, common-gate op-amps provide better gain than conventional two-stage op-amps, enhance PSRR (Power Supply Rejection Ratio), and allow for self-compensation.

Folded Common-source, Common-gate Stage Amplifier Gain Derivation

The gain derivation is performed according to Fig. 1(a) folded common-source, common-gate op-amps to select voltage $V_{b1}$and V_{b2}. The low end of the pendulum is

$$V_{OD3} + V_{OD5} \tag{1}$$

The high end of the pendulum is

$$V_{OD} - (|V_{OD7}{}^{|+|}V_{OD9}|)\cdot \tag{2}$$

Therefore, the maximum value of the swing of each side of this common-source, common-gate op-amp is

$$V_{DD} - (V_{OD3} + V_{OD5} + |_{V_{OD7}}| + |_{V_{OD9}}|)\cdot \tag{3}$$

The op-amp half of the circuit, as given in Fig. 2(a), shows that the gain is$|\mathrm{A_V}| = \mathrm{G_m R_{out}}$. So to calculate separately Gm and Rout. As in Fig. 2(b) the output short-circuit current is approximately equal to the drain current M_1， which is viewed in from the source of M_3.The impedance obtained is $\left(\frac{1}{\mathrm{g_{mb3}+g_{m3}}}\right)\|\mathrm{R_{O3}}$. Typically much lower than $\mathrm{R_{O3}}\|\mathrm{R_{O5}}$， from this it follows that $G_m \approx g_{m1}$. The output open-circuit equivalent circuit is shown in Fig. 2(c), then $\boldsymbol{R_{out} \approx R_{op}}\|[(\boldsymbol{g_{m3} + g_{mb3}})\boldsymbol{r_{o7}}(\boldsymbol{r_{o1}}\|\boldsymbol{r_{o5}})]$. From this:

$$|Av| \approx g_{m1}\{[(g_{m3}+g_{mb3})r_{o3}(r_{o1} \| r_{o5})] \| [(g_{m7}+g_{mb7})r_{o7}r_{o9}]\}$$

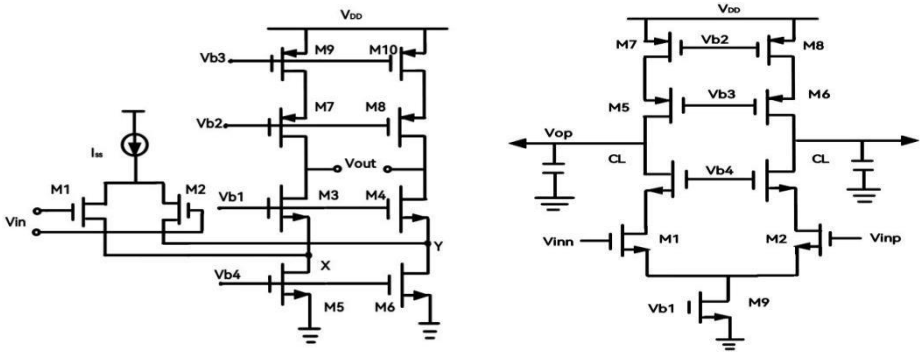

FIGURE 1. (a) Folded common-source common-gate op amp (b) Sleeve common-source common-gate op amp

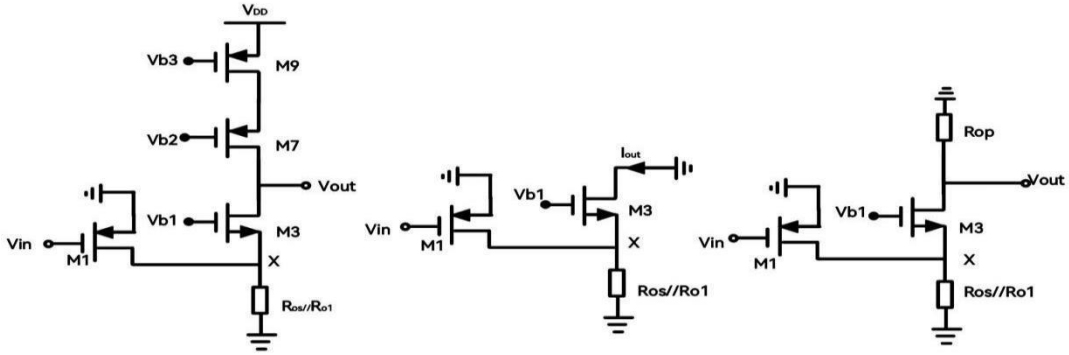

FIGURE 2. (a) Half-side circuit of folded common-source common-gate op-amp; (b) Equivalent circuit with output shorted to ground; (c) Equivalent circuit with output open-circuited

Optimization of Folded-Source Common-Gate Op-Amp Structures

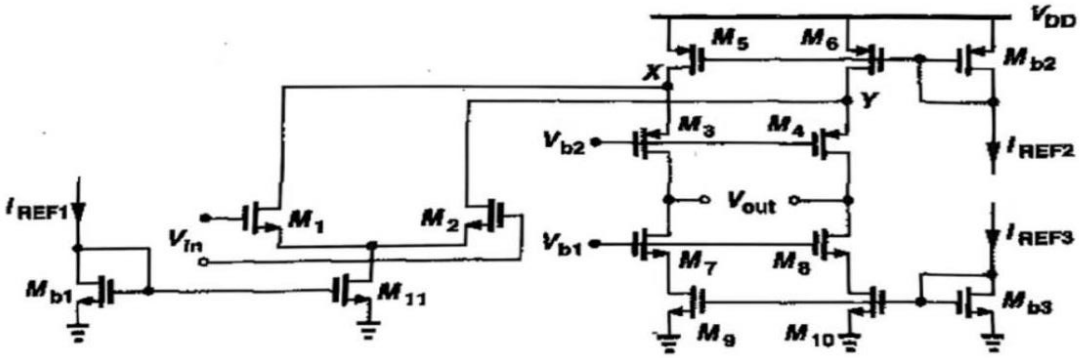

FIGURE 3. Optimization of folded common source and common gate op-amps

As in Fig. 2(a) the gain is 2-3 times smaller compared to that of a similar sleeve common source and common gate. Therefore, the circuit is optimized to obtain the circuit diagram shown in Fig. 3. Folded common-source, common-gate op amps can contain NMOS input devices and PMOS common-source, common-gate transistors. The rate of carrier migration is greater in NMOS tubes, providing greater gain to the circuit. The beauty of this is that the poles on the Fig 3 refolding points are even lower.

MISMATCH OF FOLDED COMMON-SOURCE, COMMON-GATE AMPLIFIER STRUCTURES

On the Results of the Mismatch and Dissonance Research

Extremely low-power rail-to-rail high-gain low-distortion operational amplifiers designed by Guojun Sun et al. [6]. The amplifier employs two complementary input stages over the full voltage range and is capable of cross-conducting for rail-to-rail inputs. The circuit amplification can be effectively increased by multi-stage Cascode modules. The use of a single input for the output stage effectively reduces the quiescent current of the output current as well as the mismatch of the circuit, and maintains the stability of the circuit to a certain extent. S.M. Rezaul Hasan et al. proposed a highly simplified technique for mid-frequency band analysis of source-level followers [7]. The technique is applied to the analysis of transconductance-enhanced source followers, and the accurate analysis of drain-loaded source followers is applied to the gain analysis of stacked non-ideal mismatch differential amplifiers. This approach more fully analyzes the mismatch and the gain produced by the mismatch.

Reasons for the Occurrence of Mismatches

Mismatch is the main cause of high mismatch and low CMRR (Common Mode Rejection Ratio), as well as low PSRR (Power Supply Rejection Ratio).

Manufacturing process and layout design

In general, the analysis of amplifiers assumes that the circuit is perfectly symmetrical, i.e., both sides of the circuit present devices with identical characteristics as well as bias currents. However, in the actual IC fabrication process, there is a possibility of some error in the production process of each device. Devices that are nominally identical will also have limited mismatches.

Internal properties of the device

The characteristics of MOSFETs in the saturation region are expressed as:$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$ For two transistors with the same nominal μ, C_{OX}, W, L and V_{TH} there exists a mismatch between them resulting in a mismatch in drain current (fixed), or a mismatch in gate source voltage (fixed). As A and B increase, the relative mismatch between C and D decreases, i.e., larger devices exhibit smaller mismatches. As W and L increase，the relative mismatch between $\frac{\Delta W}{W}$ and $\frac{\Delta L}{L}$ decrease.

Mismatch Analysis on Common-source, Common-gate Op Amps

The mismatch of this circuit is analyzed based on the optimization of the folded common-source, common-gate op amp of Fig.3. After comparison, it can be seen that the mismatch caused by the common source row has a greater impact on the performance of the circuit compared to the common gate tube row.

CONSTRAINTS AND DEVELOPMENT

Although the folded common-source, common-gate op-amps have a large gain, they still have some limitations. The folded structure introduces an additional current branch, which results in a significantly higher static power consumption than the sleeve common-source, common-gate op-amps, and is not perfectly adapted in some devices with low-power requirements. In addition the increase in node capacitance in the folded topology reduces the slew rate and bandwidth, which can be limiting for high-speed applications. An increase in the number of stacked transistors exacerbates noise (e.g., thermal and flicker noise) and affects the signal-to-noise ratio of high-precision systems. Therefore, the shortcomings of folded common source and common gate op-amps in terms of power consumption, speed, and noise still need to be further improved by circuit optimization design.

High-performance CMOS self-biased complementary folded common-source, common-gate operational amplifier realized by self-biased complementary folding technique [8]. Eliminates the problem of bias voltages becoming more sensitive to noise and crosstalk, and bias points becoming highly sensitive to production processes. Maximum Gain and Low Noise Achieved by Incorporating a Folded Common Source and Common Gate Circuit Structure into a New Compact, Low-Power Variable Gain Amplifier (VGA) Architecture for Multi-Standard Receivers for Wireless Communication. Maximum gain and low noise can be achieved with extremely wide gain variations, controlled dynamic gain range, low noise, and low power consumption [9]. Low-power and high-precision instrumentation amplifiers are often required in electrocardiogram (ECG) signal acquisition systems. In order to accurately acquire and amplify weak biological signals, the use of a folded common source and common gate structure in the input stage can effectively improve the common mode rejection ratio of instrumentation amplifiers [10].

CONCLUSION

In this paper, we analyze the performance advantages of folded common-source common-gate op amp, derive their gain equations, and explore the effects of mismatch generation. The results show that the folded common-source common-gate transporter op amp outperforms the conventional sleeve structure in terms of high impedance, large swing and wide common mode range, but is limited by power consumption, speed and noise performance. Future research can be carried out in the following directions: folded common source and common gate op-amps can be introduced with adaptive bias circuitry and dynamic compensation techniques to enable the optimized circuit to switch between low-power and high-swing modes to optimize the energy-efficiency ratio. Folded common-source, common-gate op-amps can be combined with advanced processes (e.g. FinFET devices) to suppress short-channel effects and enhance output impedance and gain. In addition, the potential for applications in emerging scenarios such as low-voltage, high-precision ADC or biomedical sensing will further drive their practical engineering value.

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