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Research on the Design and Performance Optimization of High-Precision Low-dropout Voltage Regulators

Yifan Su[1] and Rui Tang [2, a)]

[1]*College of Computer and Information Engineering (College of Artificial Intelligence), Nanjing Tech University, Nanjing, 210000, China*
[2]*School of Mechanical and Electronic Control Engineering, Beijing Jiaotong University, Beijing, 100089, China*

[a)] *Corresponding author: 22222016@bjtu.edu.cn*

Abstract. In modern electronics, the performance of power modules significantly impacts device performance. As the size of semiconductor devices shrink, power management circuits become crucial, yet China lags in chip technology. This study focuses on Low Drop-Out Regulators (LDOs). It explores its design and performance optimization. The designed LDO has an output voltage of 1.8V. In terms of linear adjustment rate, the performance of output voltage change rate is less than 2.75mV/V within the range of input voltage 1.8V~3.0V has been achieved; As for temperature stability, the output voltage drift is controlled within 21.1ppm/°C within a wide temperature range of -30 ° C to 120 ° C; The power suppression ratio reaches over 74dB at low frequencies. For load transient response, dynamic bias current control technology was adopted to achieve fast response characteristics with an output voltage dip of less than 10mV and a recovery time of less than 250 μ S during a 500mA load step change. At a load current of 0, IQ=139uA.These methods greatly improve the transient response performance of LDO. These technological innovations not only fill the technical gap in high-precision LDO design in China but also provide reliable technical support for the application of domestic power management chips in high-end fields such as 5G communication and automotive electronics. The research results fully demonstrate the possibility of realizing high-performance analog chips based on mature domestic processes, which has important strategic value for promoting the independent and controllable development of the domestic semiconductor industry chain.

INTRODUCTION

In the case of many modern electronic devices, the performance of the power module will directly determine the performance and normal working life of the electronic equipment [1]. Due to the different amplitude and waveform requirements of the supply voltage for each functional module within the chip, the power management circuit plays a key role in adapting to these diverse requirements. As the volume of semiconductor devices continues to decrease, more devices can be integrated on wafers of the same size, and the speed of devices can be significantly improved, the packaging volume of chips is reduced, the production cost is reduced, and finally the actual product is more lightweight and portable [2]. Nowadays, as a major manufacturing country in the world, China's domestic electronic products have established a good reputation in the domestic and foreign markets by virtue of diversified product layout and outstanding cost-effective advantages, and their performance has also been widely recognized. As the core technology of electronic products, chips, we are far from being among the world's leaders, and there is a big gap between us and countries with developed chip industries, such as the United States and South Korea [3]. Although China's power management chip industry started late and is currently facing international technical barriers led by the United States, based on the country's strategic deployment and continuous investment in the semiconductor industry, this field still shows strong development potential and broad prospects.

In 2015, Tak-Jun Oh of Kangwon National University proposed a digital LDO with transient response enhancement technology [4]. This technology effectively shortens the transient response time and suppresses voltage overshoot/undershoot in the event of sudden changes in load current. The DLDO is designed to monitor the

output voltag.e deviation and dynamically increase the loop gain when the deviation exceeds a preset threshold. In 2017, Xingyuan Tong et al. designed an LDO with fast transient response [5], which is fully integrated on-chip without off-chip capacitors, and can achieve adaptive transient current distribution during load current changes by using auxiliary transmission transistors and control circuits, so as to enhance the transient response of the circuit and reduce the output voltage jump. In the field of LDO in recent years, new research has sprung up, and more and more chips have begun to develop in the direction of total integration, in the development of LDO, many novel structures have been proposed, and all kinds of structures can improve the performance parameters of LDO to a certain extent, but due to the complexity of the device structure, it will bring the problem of reducing the overall current efficiency. In general, scholars at home and abroad mainly focus on how to improve the transient response speed of DLDO when studying DLDO. Common methods to improve transient response include analog assistance, event-driven, asynchronous control, coarse-thin double-loop control, and SAR algorithms [6].

This article studies the design and optimization of high-performance low dropout linear regulators, with a focus on addressing output accuracy, temperature stability, and transient response issues. To this end, a dynamic bias current control scheme is proposed, which uses high conversion rate error amplifiers and techniques such as controlling the power transistor base slew rate to improve its transient response.

THEORY

Low Drop Out Regulator (LDO) is a power management device used to stabilize output voltage (the structure of the circuit can be seen in figure 1), characterized by an extremely low voltage difference between input and output voltages (usually only a few hundred millivolts). It works through linear regulation and has the advantages of low noise and high precision. It is widely used in electronic devices that are sensitive to power quality, such as mobile devices and communication modules. However, its efficiency is low and it is suitable for low to medium power scenarios. LDO is mainly composed of an error amplifier (EA), a bandgap reference circuit (BG) power switch transistor, and a feedback resistor. The bandgap reference circuit generates a reference voltage VREF to the negative terminal of the amplifier, which is connected to the gate of an adjusting transistor (commonly PMOS or NMOS transistor) after the amplifier. The drain of the adjusting transistor is connected to the output. When the load current changes, it causes the output voltage to decrease

The voltage fluctuates, and the feedback network detects the output voltage fluctuation, generating a feedback voltage VFB, which is transmitted to the positive terminal of the amplifier through a feedback resistor. The amplifier amplifies the difference between VREF and VFB and sends it to the regulating tube, which then controls the regulating tube to generate current and stabilize the output voltage [7].

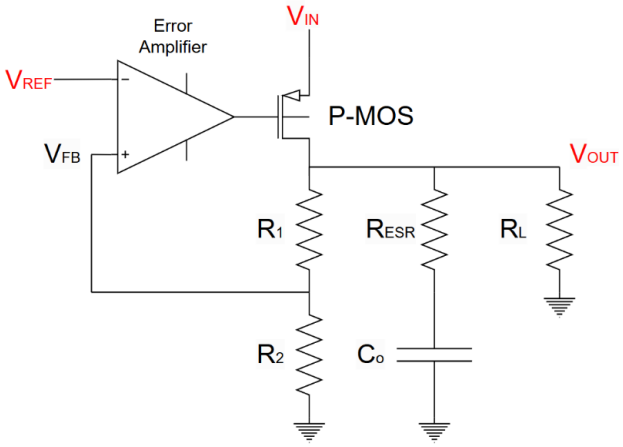

FIGURE 1. Schematic diagram of the LDO circuit

The changes to VOUT are as follows：

$$V_{FB} = V_{OUT} \times \beta \tag{1}$$

$$(V_{REF} - V_{FB}) \times A = V_{OUT} \tag{2}$$

$$V_{OUT} = \frac{A}{1+A\beta} V_{REF} \tag{3}$$

where open-loop gain A refers to the gain that includes the error amplifier and the adjustment tube as a whole. When A is big enough：

$$\frac{A}{1+A\beta} \approx \frac{A}{A\beta} \approx \frac{1}{\beta} \tag{4}$$

so:

$$V_{OUT} = \frac{1}{\beta} V_{REF} = \frac{R_1+R_2}{R_2} V_{REF} \tag{5}$$

Conclusion: When the regulator and feedback network are working properly, the output voltage is determined by the feedback network and VREF, and the output voltage is stable as long as both are stable. Under normal conditions, VREF is the only variable of the output voltage of the entire circuit.

SIMULATION RESULTS

The output voltage of the LDO in this design is 1.8V. Like the bandgap reference voltage source, the Linear Regulation Rate also reflects the ability of the output voltage of the LDO to suppress the voltage fluctuations of the power supply. However, the linear regulation is used to evaluate the ability of the LDO to maintain a stable output voltage when the supply voltage changes slowly. As shown in the figure 2, SV=3.3m/1.2=2.75mV/V.

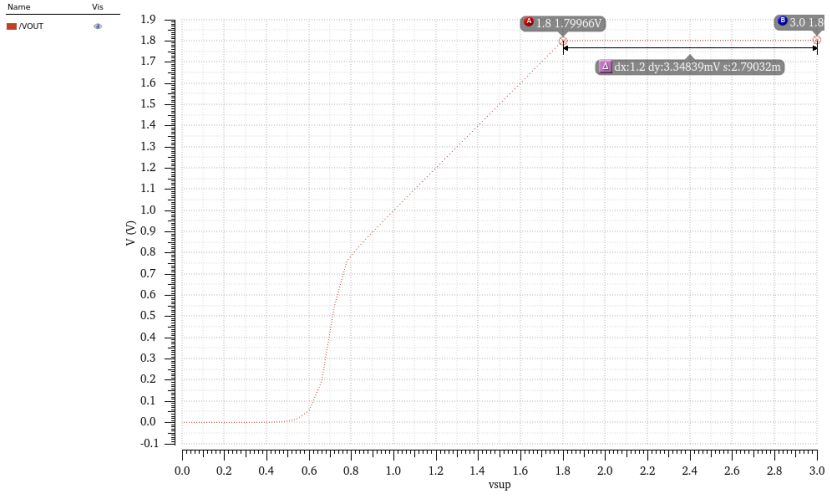

FIGURE 2. LDO voltage simulation image

The Temperature Coefficient (TC) reflects the degree to which the output voltage of the LDO fluctuates due to temperature. Since the reference voltage in the LDO circuit is provided by the bandgap reference output signal Vref, the temperature characteristics of the Vref also affect the temperature characteristics of the LDO output voltage. The smaller the Temperature Coefficient of the output voltage of LDO is, the higher the temperature independence of its output voltage will be. Conversely, the greater the Temperature Coefficient of the voltage, the lower the temperature independence of its output voltage. As shown in the following figure 3, during the variation of ambient temperature from -30.0℃ to 60 ℃, the voltage output varies by approximately 3.43mV. The calculation formula for Temperature Coefficient characteristics is as follows:

$$TC = \frac{V_{max}-V_{min}}{V_{nominal}(T_{max}-T_{min})} * 10^6 \text{（}ppm/℃\text{）} \tag{6}$$

The Temperature Coefficient is obtained as 21.1ppm/℃.

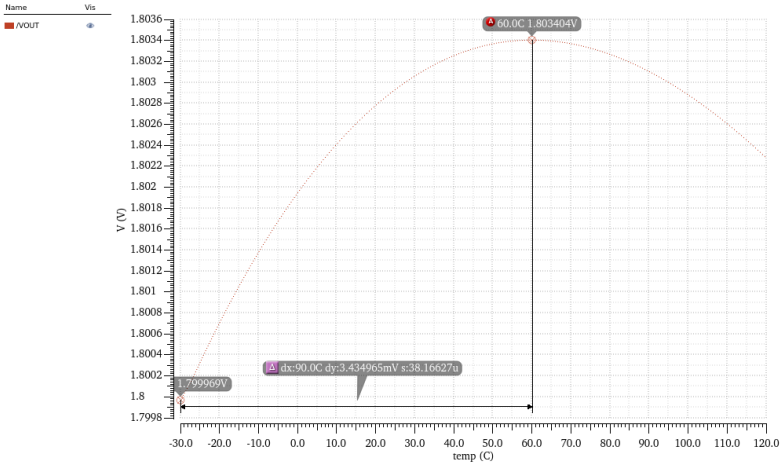

FIGURE 3. LDO temperature fluctuation image

Power Supply Rejection Ratio (PSRR) is a performance metric that evaluates the ability of the output voltage of an LDO to suppress small signal fluctuations in the supply voltage. Its mathematical expression is as follows.

$$PSRR = 20\lg\left(\frac{V_{out}}{V_{in}}\right) \tag{7}$$

Vout represents the small signal change of the LDO output voltage, and Vin represents the small signal change of the supply voltage of the LDO circuit, respectively. The unit of PSRR is usually dB, and its numerical calculation result is less than zero, and the smaller the value of the supply voltage rejection ratio, the stronger the output voltage of the LDO to suppress the AC small signal component of the supply voltage fluctuation. The PSRR of the LDO depends primarily on the PSRR of the BGR and the internal AMP.

As shown in the figure 4, the AC simulation yields PSRR=74dB at low frequency.

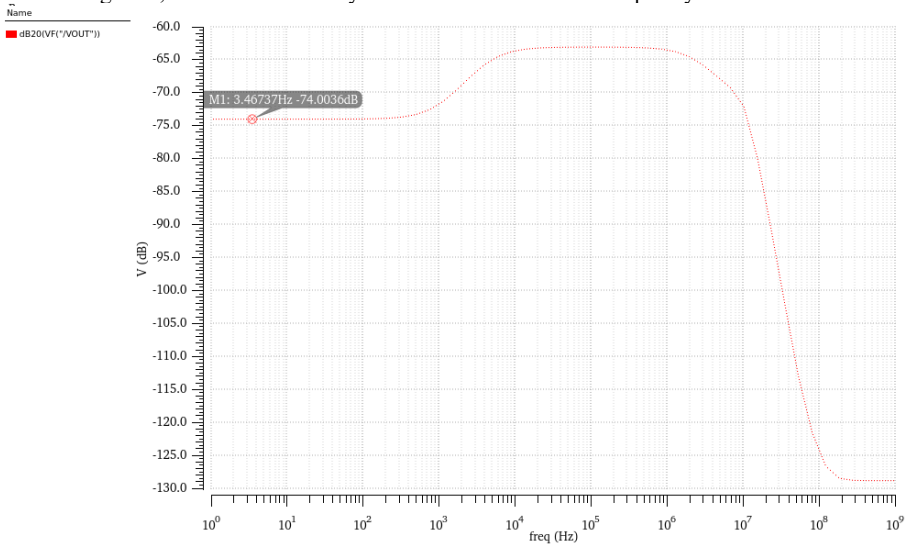

FIGURE 4. AC simulation in LDO

When the load current changes greatly and quickly, the working state of the LDO circuit will change, and the output voltage will pulse instantaneously, and it will take a certain amount of time to return to stability. By attaching a capacitor CL to the output termination of the LDO to avoid over impulsing the output voltage. When the current value provided by the LDO is greater than the current load, the ability of the capacitor CL to store the charge is used to absorb the redundant current provided by the LDO. When the current load is greater than the current provided by the LDO, the capacitor Cout will release the stored charge, thereby supplying a certain amount of current to the current load.

The figure 5 below shows the output waveform with a rapidly changing load current from 0-500mA.

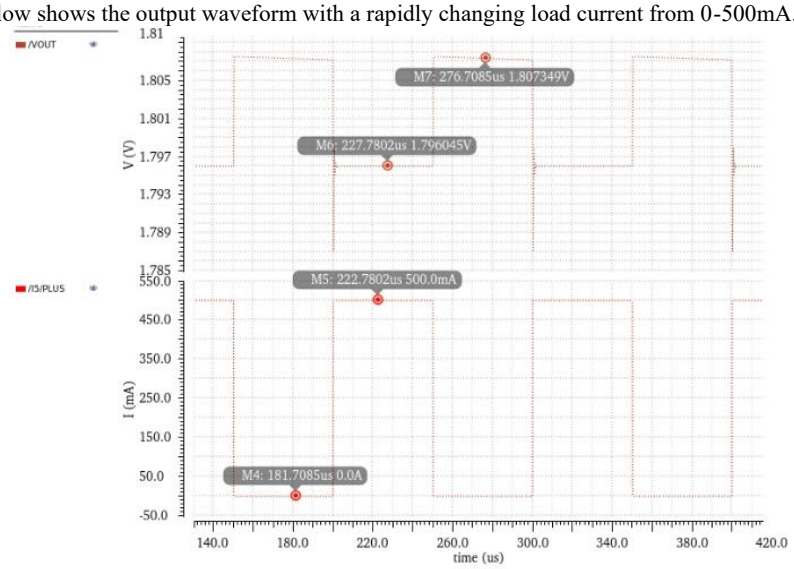

FIGURE 5. LDO load current

In figure 6 the recovery time of the output is 250us under a large current step.

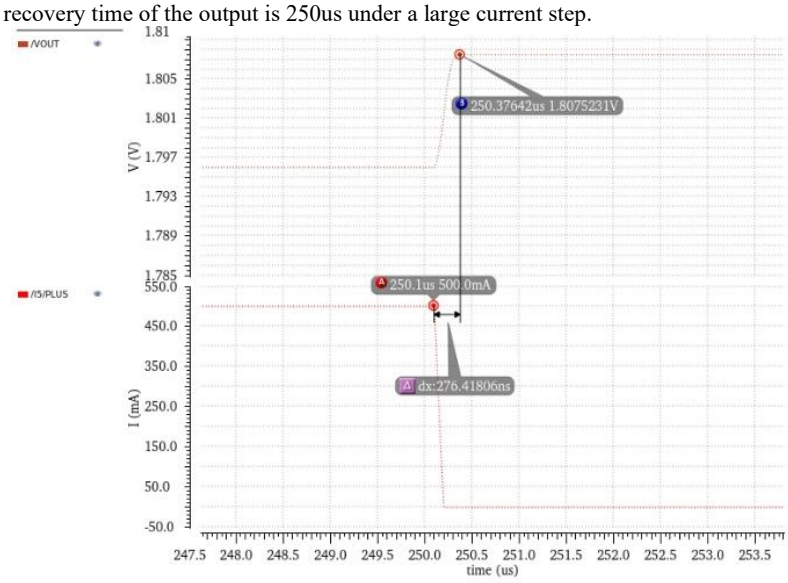

FIGURE 6. LDO current step diagram

In the case of 0 load current, the current simulation is carried out, as shown in the figure 7 IQ=139uA.

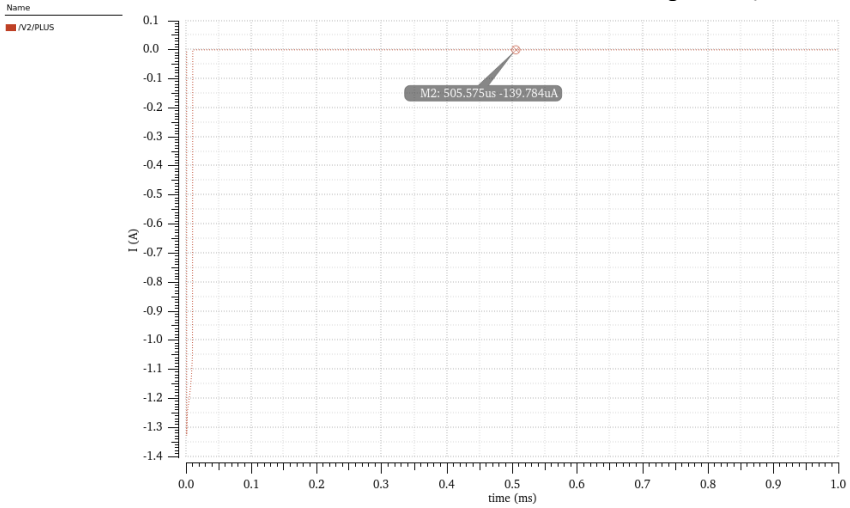

FIGURE 7. Simulation diagram of 0 current input in LDO

DISCUSSION

The transient characteristics of LDOs are usually described by the maximum change in output voltage during transient response (overshoot voltage) and the time required to reach a steady state (recovery time), and it is generally desirable that the output voltage ripple of LDO is low and can stabilize quickly during transient periods [8].

Therefore, in order to improve its transient response, the transient response of the LDO load can be improved mainly by increasing the closed-loop bandwidth of the system and enhancing the base slew rate of the adjustment tube. The optimized load transient response can use a high slew rate error amplifier to quickly charge and discharge the parasitic capacitance of the power tube. The high-voltage slew rate at the base of the power tube can make the base node voltage change rapidly in the target direction [9], so as to respond to the load transient change. Common-mode feedback is often used to increase the slew rate at the output of an op amp, but the disadvantage of using high slew rate error amplifiers is that they require high quiescent currents.

Dynamic biasing can also be used to sense changes in load current or output voltage and to adaptively bias the LDOs. For example, the comparator circuit monitors the output overshoot and undershoot and controls the bias boost circuit to increase the bias current of the LDO during transient changes to increase the bandwidth. Alternatively, circuit performance can be improved by using the slew rate of the power transistor base, which requires the ability to detect response spikes quickly and react independently of the main LDO loop to provide high currents to increase the slew rate at the power transistor base node [10].

CONCLUSION

In general, this paper focuses on the properties and transient response enhancement performance of low-dropout linear regulators (LDOs).In this article, it is designed for an output voltage of 1.8V. In terms of performance indicators, the linear regulation rate is less than 2.75mV/V, the temperature drift is less than 21.1ppm/℃, the low-frequency PSRR is 74dB. In terms of the load transient response, the response characteristics of an output voltage drop of less than 10mV and a recovery time of less than 250 μ S when the load changes step by 500mA have been achieved. The load current IQ = 139uA at 0 load current. Focusing on the transient response of LDOs, this paper proposes to optimize the slew rate by increasing the closed-loop bandwidth and adjusting the slew rate of the tube base, including using a high slew rate error amplifier, dynamic bias and slew rate boosting circuit. In modern electronic devices, power module performance affects the overall performance and operating time of the device. The development of semiconductor devices makes power management circuits more and more critical, although China

has advantages in electronic product manufacturing, but chip technology and foreign countries have a big gap. This study is of great significance to improve China's power management chip technology, break technical barriers, and promote the development of the semiconductor industry. In the future, LDOs will evolve in the direction of high performance and full integration, further optimizing transient response, reducing overshoot voltage and recovery time, and reducing off-chip components. With the emergence of emerging application scenarios, LDOs will continue to innovate in terms of low power consumption and high reliability, expand application fields, and help the development of the electronics industry. In short, LDO, as a basic linear regulated power supply, will have a vigorous development in a wider range of applications.

AUTHORS CONTRIBUTION

All the authors contributed equally and their names were listed in alphabetical order.

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