Qubit Design in Quantum Computing Hardware: Tecnologies, Challenges and Perspective

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Abstract. Quantum chips form the foundational hardware for quantum computing, promising transformative impacts across optimization, secure communications, and artificial intelligence. This paper surveys five leading qubit implementations—superconducting circuits, neutral-atom arrays, trapped ions, photonic systems, and silicon-based quantum dots—highlighting their distinct operating principles, recent milestones, and inherent trade-offs. Superconducting platforms leverage mature microfabrication to achieve hundreds to thousands of qubits with rapid gate times but require millikelvin environments and face millisecond-scale coherence limits. Neutral-atom and ion-trap architectures offer exceptionally long coherence (seconds to hours) and high-fidelity operations, making them ideal for quantum memory and precision simulation, yet scaling remains constrained by control complexity. Photonic chips excel at room-temperature operation and quantum networking via entangled photons, though deterministic two-qubit gates and on-chip integration pose challenges. Silicon quantum dots promise CMOS compatibility and sub-microsecond spin coherence, but demand atomic-scale fabrication precision and advanced cryogenic control. We analyze the tension between qubit count, error rates, and engineering practicality, and discuss emerging solutions such as hybrid integration, advanced error-correction codes, and novel materials. Looking ahead, coordinated optimization across these platforms—combining fast superconducting processors, long-lived atomic memories, photonic interconnects, and scalable silicon arrays—will be critical to transition quantum chips from research prototypes to industrially viable systems that redefine computing, communications, and AI.

INTRODUCTION

Quantum computing represents a paradigm shift in information science by leveraging the superposition and entanglement of quantum bits (qubits) to deliver exponential speedups for certain classes of problems. With its inherent parallelism, quantum hardware outperforms classical systems in areas such as cryptography, materials simulation, artificial intelligence, and complex optimization. For instance, quantum processors can dramatically accelerate large-scale search and number-theoretic algorithms. Quantum communication, which offers unconditional security, is crucial for safeguarding state secrets, corporate data, and personal privacy. Moreover, quantum accelerators hold great promise for machine learning, potentially reducing training times and enhancing model accuracy in tasks like image recognition, natural language processing, and decision-making.

The practical realization of quantum computing hinges on the underlying hardware platform. Unlike the mature, standardized architectures of classical processors, quantum chips follow diverse technological pathways—superconducting circuits, trapped ions, photonic systems, neutral atoms, and silicon-based quantum dots—each with distinct methods for qubit control, coherence properties, scalability, and environmental requirements.

Superconducting qubits, compatible with established semiconductor fabrication and offering rapid gate speeds, have scaled to the hundred- to thousand-qubit regime (e.g., IBM's Condor chip), but their millikelvin operating temperatures and millisecond coherence times pose significant engineering challenges [1]. Trapped-ion systems boast hour-long coherence and high-fidelity gates ideal for precision simulation and quantum memory, yet scaling beyond tens of qubits is hindered by the complexity of ion confinement and control [2]. Photonic chips, exploiting low-loss photon propagation, are natural platforms for quantum networks, though the weak photon–photon interactions make high-efficiency logic gates difficult to realize [3]. Neutral-atom arrays and silicon-quantum-dot devices offer prospects

for large-scale integration and room-temperature operation, respectively, but both demand breakthroughs in fabrication precision and noise mitigation [4, 5].

Despite steady progress across these platforms, two fundamental tensions remain unresolved: the balance between qubit count and fault tolerance, and the trade-off between qubit performance (coherence time, gate fidelity) and engineering practicality (cost, environmental control). For example, scaling superconducting arrays increases cryogenic complexity; trapped ions excel in fidelity but struggle with parallelism; and photonic architectures require advances in on-chip detection and integration. Moreover, the lack of a unified approach to quantum error correction exacerbates hardware fragmentation. By systematically comparing the physical principles, recent advances, and challenges of these leading platforms, this paper aims to identify the most promising technological directions for general-purpose computation, specialized simulation, and quantum networking, thereby charting a path from laboratory prototypes to industrial-scale quantum computers.

The rest of this paper is structured as follows:

Section 2 (Typical Technology Comparison and Analysis) examines five major quantum-chip platforms—superconducting circuits, neutral-atom arrays, trapped ions, photonic systems, and silicon-quantum dots—detailing their operational principles, recent breakthroughs, and performance metrics.

Section 3 (Challenge Analysis) explores the key technical bottlenecks each platform faces, including limitations in scalability, coherence-time trade-offs, and integration complexities.

Section 4 (Conclusions) synthesizes these comparative insights, delineates optimal application scenarios for each technology, and discusses the future trajectory of quantum-chip development toward commercialization and cross-domain impact.

TYPICAL TECHNOLOGY COMPARISON AND ANALYSIS

Superconducting quantum chip

The superconducting quantum chip is a chip based on superconducting circuits and quantum bits for computation, the core of which is to use the characteristic of superconducting materials so that superconducting quantum bits can be in a superposition of the ground and excited states by applying pulses and adjusting the superconducting quantum bits in an extremely low-temperature environment. The development of superconducting quantum chips, as the core carrier of the current quantum computing field, has profoundly embodied the cross-fertilization of materials science, quantum physics and micro-nano processes. In recent years, with the innovation of material system, optimization of architecture design and breakthroughs in error correction technology, superconducting quantum chips have made significant progress in coherence time, scalability and fault tolerance, and have gradually stepped forward from laboratory research to the practical stage.

The performance of superconducting quantum chips is highly dependent on the intrinsic characteristics of the materials. Early aluminum (Al)-based superconducting circuits were limited by surface oxide defects and interfacial dielectric losses, and single quantum bit coherence times were generally on the order of microseconds. In recent years, tantalum (Ta) has become a new focus due to its stable alpha-phase crystal structure and corrosion-resistant properties [1]. Studies have shown that the combination of tantalum-based films and annealed sapphire substrates can reduce surface loss to 1/2 that of aluminum-based devices, while the annealing process reduces substrate body dielectric loss by nearly an order of magnitude [1]. Tantalum thin films prepared by magnetron sputtering and high-temperature annealing processes have a superconducting transition temperature (T_c) of 4.3 K and a residual resistance ratio (RRR) of more than 55, which significantly enhances the single-photon quality factor of the microwave resonator ($Q_{int} > 3*10^7$) and lays the foundation for the realization of millisecond-scale quantum memories [1].

The electromagnetic field distribution of quantum bits directly affects the loss sensitivity. Conventional transmon structures limit further enhancement of the coherence time due to the susceptibility of the high electric field region near the Josephson junction to two-energy level system (TLS) noise [1]. To this end, novel architectures such as hairpin stripline have been proposed, whose wide-pitch design dilutes the surface electric field and combines with coaxial tunneling packaging to suppress spurious electromagnetic coupling, enabling the energy relaxation time (T_1) of on-chip quantum memories to break through 1.4 ms, approaching the performance of three-dimensional cavities [1]. In addition, tantalum airbridges (tantalum airbridges) technology realizes cross-plane signal interconnections and ground layer equalization through multilayer lithography and sacrificial layer etching processes, reduces control line crosstalk to -45 dB, and achieves 99.95% fidelity of single quantum bit gates, which provides a key support for high-density integration [6].

The scale-up of superconducting quantum chips is beginning to take shape. The IBM Condor chip integrates 1121 quantum bits, using a honeycomb layout with through-silicon vias (TSV) technology, initially demonstrating the feasibility of megabit integration [6]. The 13-bit tantalum-based processor developed by the Chinese team realizes automatic air-bridge alignment through parametric EDA tools, and achieves 99.94% and 99.2% fidelity for single-bit and double-bit gates, respectively [6]. However, scale-up still faces multiple challenges: microwave crosstalk increases due to the increase in quantum bit density, thermal load management in low-temperature systems requires nanoscale temperature control accuracy, and surface code error correction requires tens of thousands of physical bits to encode a single logical bit, which imposes stringent requirements on chip yield and power consumption [3].

Quantum error correction is at the core of practical quantum computing. Breakthroughs in it have also occurred on superconducting quantum chips. The Google team implemented the distance-7 surface code on the Willow processor and suppressed the logic error rate to 0.143% per cycle with an error suppression factor (A) of 2.14 through a neural network decoder in concert with a matching synthesis algorithm, verifying for the first time a below-threshold exponential suppression law [7]. The logic memory exceeds the optimal physical bit lifetime by a factor of 2.4 and has real-time decoding capability (63 μs latency) [7]. Meanwhile, Tencent Quantum Laboratory has found through high distance repetition code (distance-29) experiments that the logic error rate in the 10^{-10} magnitude is limited by hourly bursts of correlation errors, revealing the profound influence of material defects with potential noise sources such as energetic particle impacts [7].

Atomic Quantum Chip

Atomic quantum chip is a quantum computing platform based on neutral atoms or ions as quantum bits, and its core principle is to realize the storage, manipulation and reading of quantum information through laser manipulation of quantum states between atoms. Neutral atom quantum chip, which is based on optical tweezers technology for precise manipulation of neutral atoms, showing high scalability, has become an important breakthrough direction in the field of quantum computing in recent years, showing high scalability, long coherence time and full connectivity.

Optical tweezers can trap and manipulate neutral atoms at the submicron scale by forming arrays of potential wells with highly focused laser beams [4]. Compared to ion traps or superconducting circuits, the non-invasive nature of optical tweezers makes them more suitable for building large-scale quantum systems. With spatial light modulators (SLMs) or acousto-optic deflectors (AODs), the researchers have realized arrays containing tens of thousands of optical tweezers, such as a two-dimensional array containing 6,100 cesium atoms, with single-atom imaging fidelity of more than 99.99% and a 23-minute atom-imprisonment lifetime in a room-temperature environment [4]. This high-density, low-crosstalk architecture provides an ideal platform for quantum computing and simulation.

The coherence time of a quantum bit is a central measure of performance. Neutral atoms typically encode quantum information using ultrafine energy levels in the ground state. While conventional red detuned light traps lead to decoherence due to photon scattering and trap depth fluctuations, blue detuned bottle beam traps (BBTs) significantly reduce the photon scattering rate by imprisoning the atoms in the light intensity zero region [8]. In combination with 3D Raman sideband cooling, atoms can be prepared to a 3D kinematic ground state (phonon number close to zero), thus suppressing decoherence due to uneven phonon state distribution [8]. Experiments have shown that the quantum bit coherence time of a single cesium atom using such optimizations can be up to 20 seconds, a record for the alkali-metal atomic system [8].

Integration of large-scale quantum systems needs to overcome challenges such as optical tweezers uniformity, atomic loading efficiency and high-fidelity operation. Optimization of the SLM holographic phase by the weighted Gerchberg-Saxton algorithm enables a homogeneous array with a standard deviation of the trap depth below 12% and an atomic loading efficiency of 51.2% [4]. Furthermore, coherent transmission of quantum bits is a central requirement for partitioned architectures (e.g., storage regions separated from interaction regions). Using AOD to drive the optical tweezers to move, atoms can be transported with 99.95% fidelity over a distance of 610 microns, and in combination with dynamic decoupling techniques (e.g., XY16 sequences), a coherence time of 12.6 seconds can be sustained, which lay the foundation for parallelization of logic gates with quantum error correction [4].

A single quantum bit gate has a fidelity of 99.9834% by a global randomized benchmark, while a two-bit gate based on Rydberg interactions has a fidelity of over 99% [4]. Under the partitioned architecture, the storage area can hold thousands of atoms, which are quickly dispatched to the interaction area to perform parallel gate operations via AOD [4]. Such systems have successfully implemented applications such as quantum phase estimation, topological code structure simulation, and support mid-circuit measurement and erasure error detection.

Ion trap quantum chips

The ion trap quantum chip is a chip that uses electromagnetic fields to imprison charged ions and enables quantum computing by manipulating the ions' internal energy levels. In the rapid development of quantum computing technology, the ion trap system has gradually become one of the core routes to realize high-precision and long-life quantum processors by virtue of its unique physical properties.

The core advantage of the ion trap quantum chip stems from its ultra-long coherence time and high-precision manipulation capability. The quantum bit system, represented by ytterbium-171 ($^{171}Yb^+$) ions, has realized a leapfrog improvement in the stability of quantum states through multi-dimensional technological innovation. The research team effectively eliminates the decoherence effect of magnetically sensitive energy levels by constructing a multi-layer magnetic shielding system to suppress the ambient magnetic field fluctuations to the order of micro Gauss, combined with the static magnetic field generated by permanent magnets [2]. In microwave manipulation systems, a crystal oscillator is used as a frequency reference with a cascaded microwave switch design to reduce signal leakage by more than 160 dB, significantly reducing undesired coupling [2]. In concert, these techniques have led to a breakthrough in the coherence time of a single quantum bit from the minute level of early experiments to 5500 seconds (~1.5 hours), and to a staggering 16,000 seconds (~4.4 hours) for specific quantum states [2]. Innovations in dynamic modulation techniques further unlock the quantum bit potential. An optimization scheme based on the Knill Dynamic Decoupling (KDD) sequence successfully filters the low-frequency components of the noise spectrum by periodically applying phase-modulated microwave pulses [2]. The experimental data show that the quantum state fidelity still maintains the exponential decay feature during the storage time of 960 seconds, which provides a physical basis for the long-range evolution of complex quantum algorithms [2].

In terms of scaling, the Ion Trap system demonstrates the advantages of a unique fully-connected architecture. The latest experimental platform has realized a 30-qubit single-ion chain system, using a micromachined surface trap combined with an acousto-optic deflector (AOD) technique to accomplish high-fidelity calibration of 435 pairs of quantum bit gates with a median error rate of 4.6×10^{-4} [9]. Notably, the system introduces barium-138 ($^{138}Ba^+$) as the cooling medium through the "hybrid ion chain" design, which realizes continuous laser cooling without interfering with the computational ions, providing an innovative solution for the thermal management of large-scale systems. In application layer testing, the system successfully passed the 29 Algorithmic Quantum Bits (#AQ 29) benchmark, validating its practical potential in performing complex algorithms such as phase estimation and quantum Fourier transform [9]. In application layer testing, the system successfully passed the 29 Algorithmic Quantum Bits (#AQ 29) benchmark, validating its practical potential in performing complex algorithms such as phase estimation and quantum Fourier transform[9].

Facing the demand of practical quantum computing, the ion trap system has made important breakthroughs in the field of fault-tolerant technology. The research team achieved fault-tolerant conversion of logical quantum states between seven-qubit color codes (error-correcting distance 3) and ten-qubit codes (error-checking distance 2) by code-switching techniques [10]. The scheme utilizes flag qubits for error detection, combined with a repeated measurement strategy to suppress single-point failure propagation, and ultimately constructs a universal gate collection containing CNOT, Hadamard, and T-gates [10]. Experimental data show that the logic quantum state fidelity still exceeds 80% in a complex line containing 61 two-bit gates, verifying the operational feasibility of the system in fault-tolerant architectures [10]. This deterministic control scheme, which does not rely on magic state injection, opens up new paths for quantum computation with low auxiliary bit overhead [10].

Optical Quantum Chip

Optical quantum chip is a new type of computing chip based on photons as information carriers, which utilizes quantum states of photons, such as polarization or phase states, to represent and process information.

It is mainly developed in parallel around two major systems, Discrete Variable (DV) and Continuous Variable (CV). DV systems are based on single-photon quantum states (e.g., polarization, path encoding) and implement quantum logic gate operations through linear optical elements, but their scale-up is limited by the non-scalability of single-photon sources versus the high-precision requirements of multiphoton interference [11]. CV systems, on the other hand, take advantage of the continuous nature of the orthogonal components of the light field to construct multimode quantum resources through the deterministic preparation of compressed and entangled states [11]. Quantum microcomb technology based on silicon-based silicon nitride micro-ring resonant cavities can generate eight-mode continuous variable entangled states on a single chip and realize dynamic reconfiguration of clustered

entangled structures between supermodes through Bragg scattering effect [11]. The stability of quantum correlations with sideband frequencies up to hundreds of megahertz has been experimentally verified, laying the physical foundation for large-scale quantum state manipulation [11].

Silicon-based photonics is a core platform for integrated quantum light paths by virtue of its CMOS compatibility, and its strong third-order nonlinear effects support an efficient four-wave mixing process for on-chip quantum light sources and frequency conversion [3][11]. Lithium niobate thin film (LNOI), on the other hand, empowers high-speed quantum state modulation through strong electro-optical effects, and the modulation bandwidth breaks through the gigahertz order of magnitude [3]. Hybrid integration technology interconnects a family III-V quantum dot light source, a superconducting nanowire single photon detector (SNSPD), and a silicon optical waveguide through heterogeneous bonding to construct a fully functional quantum node [3]. For example, hybrid chips based on silicon-based modulators and aluminum phosphide lasers have achieved GHz-level quantum key distribution, with key generation rates up to two orders of magnitude higher than conventional systems [3].

In the field of quantum communication, the chip-based quantum key distribution (QKD) system compresses the device volume to the millimeter level by integrating a weakly coherent light source, a programmable optical path with a balanced zero-tap detector, and completes the hundred-kilometer-level secure key transmission in metro optical fiber networks [3]. Chip-based implementation of the Measurement Device-Independent Protocol (MDI-QKD) further eliminates security vulnerabilities at the probe side and promotes the deployment of practical quantum communication networks [3]. Quantum invisible state transfer experiments, on the other hand, have shifted from free space to integrated chips, utilizing path-polarization state conversion techniques to accomplish cross-chip quantum state transfer with fidelity that breaks through the classical limit [11].

Table.1 Summarizes the types and performance of chips.

TABLE 1. *Chip type and performance.*

Chip Type / performance	Superconducting quantum chip	Atomic Quantum Chip	Ion trap quantum chips	Optical Quantum Chip	Silicon based quantum dot chips
Scalability	kilobit grade	Currently medium, high potential	Medium (modular design)	Currently medium, high potential	tens of magnitude
Coherence time	ms	s	h	ms	b
Manipulation Speed	ns	μs	μs	μs	ns
Environmental requirements	Near absolute zero High vacuum + ultra-high cleanliness Electromagnetic shielding vibration isolation	high vacuum Optimization of optical cavity technology	Medium Vacuum mechanical stability	high vacuum Optical noise suppression	Semiconductor Process Cleanliness Material Defect Control

CHALLENGE ANALYSIS

Silicon based quantum dot chips

Silicon-based spin quantum bits specifically refer to quantum bits formed by utilizing bound electrons (holes) in quantum dots on a silicon-based substrate or by encoding the spin quantum state of the nucleus. It serves as the core carrier of semiconductor quantum computing, and has made significant progress in recent years in the areas of material design, quantum manipulation and integration processes, showing potential for scale-up applications [5][12]. In terms of materials and device design, researchers have significantly reduced nuclear spin noise in silicon-based substrates through isotope purification techniques, improving the coherence time of electron spin quantum bits from early tens of nanoseconds to hundreds of microseconds [5]. For example, the use of 28 Si-rich heterojunctions (e.g., Si/SiGe) can effectively suppress nuclear spin uplift, while the combination of micro-magnet structures to enhance spin-orbit

coupling has realized the electric dipole spin resonance (EDSR) technique, which has enabled single-bit manipulation speeds exceeding 10 MHz with fidelity exceeding 99.9% [5]. In addition, by optimizing the quantum dot barrier design and dynamic decoupling technique, the fidelity of two-bit logic gates (e.g., CZ gates) breaks through 99%, which reaches the error tolerance threshold of the surface code error correction scheme, marking the step of the silicon-based system into the practical stage [5].

Breakthroughs in process integration and cryogenic control technologies have further advanced the field. Conventional quantum chips rely on room-temperature electronics to connect extremely low-temperature quantum bits via long cables, leading to signal degradation with a surge in cooling load [12]. In recent years, heterogeneous integration technology has realized low-noise amplifiers and routing circuits at low temperatures of 4 K with an order of magnitude lower power consumption than conventional CMOS by embedding III-V high electron mobility transistors (HEMTs) with superconducting niobium (Nb) interconnect layers directly into silicon-based chips [12]. This "monolithic integration" scheme not only solves the wiring problem in multi-bit expansion, but also significantly improves the signal transmission efficiency, which provides a hardware basis for the cooperative control of a thousand quantum bits system [12].

Superconducting quantum chip

The scale-up of superconducting quantum chips still faces multiple challenges: microwave crosstalk increases due to the increase in quantum bit density, thermal load management in low-temperature systems requires nanoscale temperature control accuracy, and surface code error correction requires tens of thousands of physical bits to encode a single logical bit, which imposes stringent requirements on chip yield and power consumption [7]. At the same time, it needs to operate at extremely low temperatures close to absolute zero (about -273°C), relying on expensive dilution chillers, which significantly increases system costs and maintenance difficulties.

Atomic Quantum Chip

Efficient detection of quantum states of neutral atoms is not yet mature, and signal extraction is difficult, leading to limited computational efficiency. Relying on laser cooling and imprisonment techniques, complex optical systems are needed to control the atomic arrays, and integration is difficult. Currently there are more laboratory results (e.g. Harvard University 48 logic quantum bit model), but stability and scale production have not yet been broken through.

Ion trap quantum chips

Coulomb repulsion between ions leads to chaotic array alignment, making it difficult to scale up on a large scale (currently up to 32 bits only). Secondly, it relies on vacuum environment and high-precision laser manipulation, which requires a large number of macroscopic optical components and makes it difficult to realize chip-level integration. Ion manipulation needs to be carried out one by one, and the parallel computing ability is weak, which limits the practical application scenarios.

Optical Quantum Chip

Difficulty in realizing nonlinear interactions between photons leads to difficulties in constructing quantum logic gates, which need to rely on complex optical devices (e.g., micro-ring resonant cavities). Photonic line design requires high-precision optical components (e.g., beam splitters, couplers), and the yield and stability of large-scale integrated photonic chips are still awaiting breakthroughs. Currently, it is mainly applied to specific tasks such as bosonic sampling, and the general quantum computing capability has not yet been verified.

Silicon based quantum dot chips

The quantum state of silicon-based quantum dots is susceptible to material defects and nuclear spin noise, and the decoherence time is much lower than that of superconducting or ion trap systems. As such, the manipulation accuracy is insufficient, requiring precise control of the charge or spin state of the quantum dots, and the current single- and two-bit gate fidelity falls short of the fault-tolerant thresholds.

CONCLUSIONS

In this survey, we have compared five leading qubit technologies—superconducting circuits, neutral-atom arrays, trapped ions, photonic systems, and silicon-based quantum dots—highlighting each platform's unique strengths and persistent challenges. Superconducting qubits excel in integration density and gate speed but demand cryogenic operation and face coherence-time limits. Neutral-atom and ion-trap architectures deliver exceptionally long coherence and high-fidelity control, yet their scaling is constrained by optical complexity and trap engineering. Photonic chips offer room-temperature networking and secure communication but require breakthroughs in deterministic two-qubit interactions. Silicon quantum dots promise CMOS compatibility and rapid spin manipulation, though they hinge on atomic-scale fabrication and advanced cryogenic electronics. Across all modalities, the central tension remains between scaling qubit numbers and maintaining low error rates under practical engineering constraints. Moving forward, hybrid systems that combine fast superconducting processors, long-lived atomic memories, photonic interconnects, and scalable silicon arrays could leverage complementary advantages. Advances in materials science, error-correction protocols, and integrated control electronics will be pivotal. Over the next decade, coordinated optimization across these platforms is expected to transition quantum chips from research prototypes into robust, industry-ready devices that will redefine computing, secure communications, and AI.

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