Technological Progression of GaN RF Devices: from Crystalline Growth Engineering to Electronic Performance Optimization

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Abstract. Radio frequency (RF) technology has become an integral part of daily life, powering a wide range of applications from wireless communication devices to smart home systems. With the continuous advancements in semiconductor technology, the remarkable advantages of Gallium Nitride (GaN) in next-generation RF applications have increasingly come to light. GaN's superior electron mobility, high breakdown electric field, and excellent thermal conductivity make it an ideal choice for high-frequency, high-power RF devices. To achieve high-quality GaN materials growth, it is crucial to tackle the issues of lattice mismatch and thermal mismatch, which can lead to defects and degrade material performance. Moreover, by addressing problems such as non-uniform doping and reducing surface roughness through targeted process optimization, even better material quality can be obtained. In the structural design of GaN RF devices, various challenges, including short-channel effects (manifested as increased subthreshold current and elevated output conductance), gate leakage current, current collapse, and reduced breakdown voltage, must be carefully and rationally addressed. Only by effectively mitigating these issues can the performance of RF devices be optimized, thus significantly enhancing their operational efficiency and reliability.

INTRODUCTION

Radio frequency (RF) refers to oscillating electromagnetic waves within the range of 3 KHz to 300 GHz. RF technology has extensive applications in daily life, including contactless smart cards, electronic tags (RFID), and electronic barcodes. With the developments in semiconductor technology, people have been realizing the advantages of gallium nitride (GaN) in next-generation radio frequency (RF)applications. The band gap of gallium nitride(GaN)is 3.39ev, and as a wide band gap semiconductor(material wide-bandgap semiconductors, also referred to as WBG semiconductors or WBGS, are semiconductor materials that exhibit a wider bandgap than conventional semiconductors), GaN exhibits high mechanical stability and thermal conductivity in its crystalline structure, enabling exceptional performance retention under high-frequency, high-voltage, and high-temperature operating conditions. Compared with silicon-based radio frequency (RF)electronic devices, GaN demonstrates superior performance at elevated operating frequencies, enabling its particular suitability for high-power, high-frequency RF applications where stringent operational demands must be met. Therefore, in the field of RF electronics, GaN materials are getting attentions of reseachers [1]. However, due to the limitations of current technology, the development of GaN materials is still facing various challenges. Firstly, there remains critical challenge of achieving high-quality material growth. The quality of materials determines the stability of devices and the upper limit of their performance. Secondly, in terms of device performance, the structural design of GaN HEMT devices is a crucial decision. The structural design of the device determines its performance, which in turn determines its application. And the structual design desides the fundamental performance characteristics of the HEMT devices, which in turn govern its viable application domains. This review summarizes the research involving the selection of diverse substrates, advancements in epitaxial methodologies, and innovations in doping techniques; and changing HEMT device parameters such as gate-drain spacing and gate length, HEMT device structures including the

presence or absence of field plates and substrate composition, as well as methods to proportionally scale down HEMT devices. These studies aimed to achieve high-quality crystalline growth and HEMT device optimization.

EVOLUTION OF GAN MATERIAL GROWTH TECHNOLOGY

GaN material growth methods encompass both heteroepitaxy and homoepitaxy. Heteroepitaxy emphasizes substrate selection but faces challenges such as lattice mismatch and thermal expansion coefficient mismatch. Homoepitaxy (GaN-on-GaN), while offering superior crystalline quality, suffers from prohibitively high substrate costs. For GaN materials, various growth techniques exist. Although researchers have conducted extensive exploration on bulk single crystal growth of GaN, the bulk single crystal growth process has not yet been fully optimized. Currently, the acquisition of high-quality GaN materials (or other group III nitrides) primarily relies on heteroepitaxy, because of the limination of the GaN substrate [2][3]. GaN heterostructures can induse two-dimensional electron gas with high surface density and high electron mobility without intentional doping, thanks to the spontaneous and stain-induced polarization [4][5], and related power devices have been widely studied [3]. Therefore, material growth technology plays a crucial role in enhancing the performance of GaN RF devices. Achieving high-quality material growth requires selecting substrates compatible with high-power and high-frequency applications, as well as adopting high-throughput and low-cost epitaxial methods. However, the material growth technology is now facing many challenges, including the material surface cracks, high-denisity defects, and the high dislocation denisty caused by the substantial lattice constant mismatch and thermal expansion coefficient difference. The following section introduce methods of substrates selection and epitaxial methods to address these problems.

Substrates selection

Substrate selection is the primary consideration in material growth technology, and it's a simple and effecitive way to reduce the device temperature. Nowadays, three kinds of substrates are commonly used, which are sapphire, SiC, and Si [3].

Among these substrates, silicon (Si) substrates offer the most significant cost advantages. However, the substantial lattice constant mismatch (17%) and thermal expansion coefficient difference (56%) between GaN and Si introduce significant tensile stress in the GaN layer, leading to surface cracks [6]. To address these challenges, researchers such as Gong Xiaoliang and Chen Jianwu adopted a multi-buffer layer structure (AlN/AlGaN) combined with a low-stress AlN interlayer technology. This approach successfully enabled the growth of 100 mm (4-inch) crack-free GaN epitaxial material on standard-thickness Si (111) substrates [7]. Experimental results demonstrated that optimized thickness ratios of the AlN/AlGaN layers and the low-stress AlN interlayer effectively controlled stress distribution [7]. The crack-free GaN layer achieved a thickness of 1.6 μm with good crystal quality and surface roughness below 2 nm [7]. Electrical characterization of the HEMT epitaxial wafers confirmed that the GaN material grown on Si substrates meets the quality requirements for device fabrication [7].

Sapphire is currently the most widely used substrate material. However, the lattice mismatch between sapphire and GaN is as high as approximately 17%, resulting in high-density defects in the epitaxial materials [8]. Nevertheless, scientists have discovered that silicon carbide (SiC), which shares the same hexagonal crystal system as GaN and exhibits close lattice constants, serves as an excellent substrate for high-quality GaN epitaxial growth. Researchers such as Yu Mingjian and Xu Mingsheng employed high-resolution X-ray diffraction (HRXRD) to analyze the relative orientation, lattice constants, stress distribution, and dislocation density of GaN epitaxial films grown via metal-organic chemical vapor deposition (MOCVD) on SiC substrates, validating this perspective [9]. Their analysis revealed that GaN and SiC share identical α-axis orientations [9]. The GaN epitaxial layer demonstrated a relaxation degree exceeding 90%, with lattice constants closely matching those of bulk GaN. Compressive stress was observed in the GaN layer, while dislocation densities in the SiC substrate and GaN epitaxial layer were measured on the order of 10^7 and 10^8 cm^{-2}, respectively.

Furthermore, scientists have identified alternative methods to reduce the high dislocation density caused by lattice and thermal mismatches between sapphire substrates and epitaxial films during heteroepitaxial growth. In the study by An Xia and Xu Shengrui, argon (Ar) ion pretreatment was applied to sapphire substrates to induce nucleation, significantly lowering the dislocation density in GaN epitaxial layers. By optimizing the Ar ion implantation dose, it was found that at a dose of 1×10^{11} cm^{-2}, the screw dislocation density reached 5.26×10^7 cm^{-2} and the edge dislocation density was 1.95×10^8 cm^{-2} [10]. The total dislocation density was reduced by 65%

compared to GaN grown on conventional sapphire substrates [10]. Photoluminescence (PL) characterization demonstrated enhanced optical performance in the nucleation induced GaN epitaxial layers, with a 152% increase in PL intensity relative to untreated samples.

According to the studies, rational thickness optimization of AlN/AlGaN multilayers combined with a low-stress AlN interlayer enables effective stress modulation. This approach achieves crack-free GaN layer growth on Si substrates with a thickness of 1.6 μm, excellent crystal quality (XRD FWHM < 300 arcsec), and surface roughness below 2 nm (AFM RMS). Additionally, Ar^+ ion pretreatment of sapphire substrates for nucleation induction significantly reduces dislocation density in GaN epitaxial layers (from ~10^9 to 10^7 cm^{-2}). These methodologies systematically address issues arising from lattice mismatch ($\Delta a/a$ ~17% for GaN/Si) and thermal mismatch (CTE difference ~54%).

Breakthroughs in Epitaxial Methods

Currently, mainstream epitaxial growth techniques primarily include Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE). To mitigate the lattice mismatch between Si substrates and GaN, AlN nucleation layers and AlGaN stress-relief layer structures are commonly employed. Due to the distinct lattice structures between silicon (Si) substrates and aluminum nitride (AlN), AlN layers directly grown on Si via MOCVD exhibit rough surfaces and poor crystal quality. To address this issue, scientists have adopted the strategy of introducing interlayers to mitigate the influence of Si substrates. For instance, Feng Yuxia et al. from Peking University introduced a monolayer of graphene on Si substrates, followed by NH_3 pretreatment. The sp^3-hybridized C–N bonds induced AlN nucleation, thereby optimizing the crystal quality of GaN epitaxial layers [11]. Similarly, Bessolov et al. demonstrated that depositing a 50 nm thin SiC layer on Si substrates, followed by epitaxial growth of 20 nm AlN and 1 μm GaN, significantly alleviated the high dislocation density caused by lattice mismatch between Si and GaN. This approach enabled the fabrication of high-quality GaN epitaxial layers [11].

In the MOCVD growth of GaN thin films, H_2 is typically used as the carrier gas to transport the Group III source, $Ga(CH_3)_3$ (trimethylgallium, TMG), and the Group V source, NH_3, into the reaction chamber. The source gases undergo a series of chemical reactions, including pyrolysis and adduct formation, ultimately forming GaN thin films on the high-temperature substrate. However, due to the presence of gas-phase parasitic reactions, a portion of the precursor gases is converted into harmful nanoparticles, which not only reduces the utilization efficiency of the source gases but also compromises the quality of the thin films. Therefore, investigating the gas-phase reaction pathways of GaN will contribute to enhancing both the quality and growth rate of thin films. By separately investigating two scenarios—the adduct reaction between TMG (trimethylgallium) and one NH_3 molecule (Model 1) and the adduct reaction between TMG: NH_3 and a second NH_3 molecule (Model 2)—scientists such as He Xiaokun and Zuo Ran compared the concentrations of key reaction precursors near the substrate surface under both conditions [12]. Through this analysis, they concluded that the gas-phase reaction pathway in GaN MOCVD growth is significantly influenced by the adduct reaction involving the second NH_3 molecule [12].

Metal-Organic Vapor Phase Epitaxy (MOVPE) has been successfully employed to fabricate GaN-based MESFETs, MODFETs, UV detectors, and high-brightness blue LEDs. However, nitride-based devices grown by Molecular Beam Epitaxy (MBE) have not yet achieved comparable performance levels. However, due to the higher purity of GaN materials grown by MBE technology and its lower growth temperature (resulting in reduced thermal damage), MBE has garnered widespread attention in the scientific community. Challenges in MBE-grown GaN include low growth rates (0.04–0.15 μm/h), ion damage from nitrogen plasma sources, and inadequate monitoring of reactive nitrogen species during epitaxial growth [13]. M.A.L Johnson et al. (North Carolina State University) addressed the challenges of lattice mismatch and high dislocation density in GaN heteroepitaxy by employing homoepitaxial MBE growth on MOVPE-pregrown GaN/SiC substrates (3 μm GaN buffer layer on 6H-SiC). By replacing conventional ECR plasma with an rf nitrogen plasma source (150–400 W, N_2 pressure: 5×10^{-6}–4×10^{-4} Torr), they mitigated ion damage and achieved GaN films with dislocation densities $<10^8$ cm^{-2} (Fig. 1) and structural/optical quality comparable to MOVPE-grown GaN, evidenced by narrow XRD (0002) rocking curve FWHM of 156 arc-sec and room-temperature PL band-edge emission at 3.409 eV (FWHM = 29.7 meV) [14]. J. Ren and J.A. Edmond (Cree Research) resolved interfacial contamination issues via He/H_2 plasma cleaning and annealing (600–800°C) of GaN/SiC substrates, enabling clean MBE homoepitaxy [14]. Additionally, $Al_xGa_{1-x}N$ films (x ~0.06–0.08) and $Al_xGa_{1-x}N$/GaN multi-quantum-well (MQW) structures were grown by MBE, demonstrating strong PL emission at 3.62–3.69 eV and a 36 meV blue shift in GaN quantum wells due to quantum

confinement and strain effects [15]. These results validate MBE as a viable method for high-quality nitride epitaxy, particularly for UV optoelectronic applications [15].

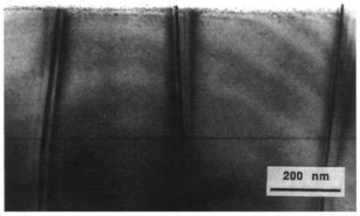

Figure.1. MBE-grown epilayer on MOVPE-grown GaN buffer layer with proper surface cleaning [16].

In summary, the poor growth quality of GaN films grown on Si substrates via MOCVD, caused by the lattice mismatch between GaN and Si, can be addressed by introducing an intermediate layer.In the MOCVD growth of GaN thin films, parasitic gas-phase reactions involving NH_3 can occur, leading to degraded film quality. These reaction pathways are significantly influenced by adduct reactions involving a second NH_3 molecule.Interface contamination issues in GaN/SiC substrates can be effectively addressed through He/H_2 plasma cleaning combined with annealing (600–800° C), enabling clean MBE homoepitaxy.

Innovations in Doping Technology

Doping is also a crucial technique for the growth of high-quality materials. M.Amilusik et al. (Institute of High-Pressure Physics, Polish Academy of Sciences) conducted five HVPE growth experiments to address the non-uniform silicon (Si) doping and free carrier gradients in GaN crystals. By systematically varying the HCl flow rate (HCl^{dop}) in the dichlorosilane (H_2SiCl_2) precursor line, they optimized Si incorporation, achieving concentrations up to 10^{19} cm^{-3} [16]. Through secondary ion mass spectrometry (SIMS) and Raman spectroscopy (RS), they identified that Si gradients along the [0001] growth direction stemmed from Si deposition within the reactor and morphological evolution during growth (e.g., step-flow to hillock-dominated modes). The team demonstrated that increasing HCl^{dop} enhanced Si doping efficiency but could not eliminate gradients, which were mitigated by growing on as-grown HVPE-GaN substrates, reducing dislocation densities to $<10^8$ cm^{-2}<$10^8$$cm^{-2}$ [17]. Their stress model linked doping non-uniformity to surface kinetics, validated by hyperspectral Raman mapping showing minimized biaxial stress (−0.12 GPa−0.12GPa) in the top GaN layer [16，17].

In 2023, Kumar et al. experimentally demonstrated that increasing Mg doping concentration leads to deterioration of GaN crystal quality and enhanced surface roughness [19]. Therefore, while maintaining p-type doping concentration, optimizing crystal surface quality and controlling roughness remain critical challenges requiring focused attention. In experiments conducted by Gao Nan, Fang Yulong et al., the delta-doping technique enabled balanced optimization of p-type GaN material properties—achieving controlled doping concentration while simultaneously reducing surface roughness and dislocation density—through precise regulation of temperature, pressure, and TMGa pulse duration during doping, under fixed Cp2Mg precursor supply conditions [20]. The results demonstrate that samples grown at 1150°C with a chamber pressure of 400 mbar (40,000 Pa) and TMGa injection time of 40 s exhibit an RMS surface roughness of 0.643 nm, (002) plane FWHM of 176.8 arcsec, hole mobility of 11.8 $cm^2/(V·s)$, and hole concentration of $1.02×10^{18}$ cm^{-3}, achieving balanced optimization of electrical properties and crystalline quality [20].

In summary, by systematically adjusting the flow rate of HCl in the dichlorosilane precursor, the issues of non-uniform Si doping and free carrier gradients in GaN crystals can be resolved. In Delta doping experiments, the balance between doping concentration, surface roughness, and dislocation density in P-type GaN materials can be optimized by controlling temperature, pressure, and the duration of TMGa introduction during the doping process.

OPTIMIZATION OF GAN HEMT-BASED DEVICES

Currently, the major challenges faced in the structural design of GaN RF devices include short-channel effects caused by reduced gate length (encompassing issues such as increased subthreshold current and elevated output conductance), as well as gate leakage current, current collapse, and reduced breakdown voltage. Currently,

the gate length of GaN HEMT devices has been scaled down to the nanometer regime, leading to pronounced short-channel effects manifested as reduced gate modulation efficiency, threshold voltage shift, and increased output conductance. These phenomena will severely degrade the electrical performance and frequency characteristics of GaN HEMT devices, potentially rendering the devices inoperable [21]. The following section summarizes two approaches developed by scientists to mitigate short-channel effects, both of which have enhanced the performance of GaN RF devices. Additionally, the combination of surface passivation technology with a MIS (Metal-Insulator-Semiconductor) gate structure can be implemented, serving dual functions as a surface passivation layer to suppress current collapse while simultaneously acting as a gate dielectric to mitigate gate leakage current and enhance breakdown voltage. The following section summarizes experiments conducted by scientists employing GaN surface passivation deposition technology to mitigate current collapse, gate leakage current, and related phenomena. Additionally, the implementation of a field plate (FP) structure not only significantly enhances device breakdown voltage but also effectively suppresses current collapse effects, thereby improving power density, power-added efficiency (PAE), and associated gain characteristics, while offering straightforward integration within standard fabrication processes. The following section also summarizes the improvements in gate lag current collapse and breakdown voltage degradation achieved by scientists employing field-plated (FP) AlGaN/GaN HEMTs and micro-tapered field plates.

Gate Structure Design

To enhance the device performance, the continuous scaling down of gate length has led to increasingly pronounced short-channel effects (SCEs), including elevated subthreshold current and enhanced output conductance. Furthermore, as the gate length approaches the nanometer scale under high-frequency operating conditions, the emergence of the skin effect results in substantial gate resistance, thereby limiting the improvement of the maximum oscillation frequency (f_{max}) [22]. In 2012, Zhou et al. conducted a groundbreaking comparative investigation of T-gate and Y-gate configurations to address these technical challenges [23]. The implemented HEMT structure featured an $Al_{0.3}Ga_{0.7}N/GaN/Al_{0.04}Ga_{0.96}N$ dual heterojunction design, where the $Al_{0.04}Ga_{0.96}N$ layer served as a back-barrier for short-channel effect (SCE) suppression, while the high-aluminum-content $Al_{0.3}Ga_{0.7}N$ barrier layer optimized two-dimensional electron gas (2DEG) density, complemented by a GaN cap layer for enhanced barrier potential. Characterization results revealed that T-gate architectures effectively mitigated current collapse but suffered from frequency response degradation. Conversely, Y-gate devices demonstrated simultaneous enhancements in both cutoff frequency (f_T = 120 GHz) and maximum oscillation frequency (f_{max} = 180 GHz), along with improved output power density (3.2 W/mm) and power-added efficiency (PAE > 65%). These advancements stem from the Y-gate's reduced physical gate length ($L_g \approx 85$ nm) and lower parasitic capacitance ($C_{par} \approx 12$ fF/μm), as systematically verified through RF S-parameter analysis and time-domain reflectometry measurements.

Currently, the gate length of AlGaN/GaN HEMT devices has been scaled down to the nanometer regime, leading to pronounced short-channel effects (SCEs). These effects manifest as reduced gate modulation efficiency, threshold voltage shift, and increased output conductance, which severely degrade the electrical performance and frequency characteristics of AlGaN/GaN HEMT devices, ultimately compromising their operational reliability [24-25]. Currently, on the one hand, short-channel effects can be suppressed by increasing the aspect ratio (the ratio of gate length to the distance between the metal gate and the two-dimensional electron gas (2DEG) channel) [24,26]; on the other hand, short-channel effects can be suppressed by enhancing the confinement characteristics of the two-dimensional electron gas (2DEG) in the channel [27]. In the experiments conducted by Xiao Yang, Zhang Yichuan et al., recessed etching technology was employed to enhance the device aspect ratio by fabricating trench structures [21]. Their findings demonstrated that the recessed-gate configuration significantly improves device performance: the subthreshold swing (SS) decreased from 140 mV/dec to 95 mV/dec, and the on/off ratio increased from 10^6 to 10^7 for devices with a 100-nm gate length [21]. The recessed-gate configuration demonstrates significant suppression of short-channel effects (SCEs). At a drain-source voltage (V_{DS}) of 20 V, the 100-nm-gate-length recessed-gate device achieves cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) values of 65.9 GHz and 191 GHz, respectively, representing 5.78% and 4.49% improvements compared to conventional planar-gate structures [21]. Therefore, the recessed-gate configuration effectively suppresses SCEs and enhances the frequency characteristics of the device.

Deposition Passivation

Currently, the deposition of dielectric materials via PECVD (Plasma-Enhanced Chemical Vapor Deposition) and LPCVD (Low-Pressure Chemical Vapor Deposition) has achieved significant improvements in mitigating current collapse, gate leakage current, and related issues. In 2016, ZHANG et al. utilized LPCVD-deposited Si_3N_4 as the gate dielectric layer and surface passivation layer to fabricate MIS-HEMT devices [28]. The devices exhibited a breakdown voltage as high as 1162 V, reverse and forward gate leakage currents as low as 10^{-11} A/mm, a static on-resistance (R_{on}) of 2.88 mΩ·cm², a dynamic on-resistance under 600 V drain bias stress in the off-state that only increased to 4.89 mΩ·cm², and a device figure of merit (FOM) of 469 MW • cm² [28].

However, due to inherent limitations in PECVD and LPCVD technologies that partially constrain the post-passivation device performance, researchers have proposed novel dielectric material deposition methods to further enhance device characteristics. In 2014, TOMER et al. adopted ICP-CVD (Inductively Coupled Plasma Chemical Vapor Deposition) to deposit SiN for passivation [29]. By reducing the radiofrequency (RF) power to attain low ion energy, they thereby diminished ion-induced surface damage [29]. The fabricated devices exhibited a reduction in gate leakage current to 1/40th - 1/60th of that observed in conventional PECVD-deposited SiN-passivated devices [29]. In 2020, KANG et al. optimized the SiN passivation process using a Cat-CVD (Catalytic Chemical Vapor Deposition) system, which improved the current collapse phenomenon [30]. By adjusting process parameters including gas pressure, flow rate, and catalyst temperature, they obtained dense SiN films with a refractive index of 2.12, film density of 2.7 g/cm³, and breakdown field strength of 8.2 MV/cm [30].

In summary, although PECVD and LPCVD deposition of dielectric materials have achieved significant success in improving current collapse and gate leakage current, their inherent limitations have led to the adoption of ICP-CVD-deposited SiN for passivation, reducing surface damage to the device.

Field Plate

The breakdown voltage issue, arising from the surface terrace of the barrier layer and directly associated with polarization charges and band structure at the heterojunction interface, has become a central research focus in current investigations of GaN HEMT device architectures. Currently, the gate lag current collapse issue is typically addressed by depositing passivation layers between the gate and drain in GaN HEMT devices (mentioned in 3.2), although this approach compromises breakdown voltage performance. Researchers have demonstrated that implementing field plate structures significantly enhances device breakdown voltage while simultaneously suppressing current collapse effects, thereby improving power density, power-added efficiency (PAE), and associated gain characteristics in semiconductor devices. Wei Wei, Lin Ruobing, et al. investigated the current collapse suppression capabilities of passivated AlGaN/GaN HEMTs with varying field plate dimensions under different drain bias conditions [31]. Experimental results revealed that the current collapse suppression capability of passivated devices significantly degraded with increasing drain bias. Intriguingly, at elevated drain biases, field plate dimensions exerted notable impacts on collapse mitigation efficacy, while optimized field plate configurations demonstrated consistent current collapse suppression across the entire drain bias range [31].

Beyond the breakdown voltage degradation induced by passivation layers, researchers have found that while scaling down device dimensions facilitates enhanced high-frequency performance in GaN-based HEMTs, this miniaturization inevitably triggers internal electric field crowding, consequently compromising breakdown voltage characteristics. To address these challenges, the implementation of a novel micro-tapered gate field plate architecture enables significant improvement in breakdown voltage while maintaining frequency response characteristics, achieving critical performance trade-off optimization in GaN HEMT devices. Huang Zhentong, Mi Minhan, and others conducted simulation analysis on AlGaN/GaN HEMTs with different critical parameters (tilt angle), systematically studying the influence of different tilt angles on device characteristics [32]. The study found that the breakdown voltage (V_{BE}) increases as the tilt angle decreases, whereas the current cutoff frequency (f_T and maximum oscillation frequency (f_{max}) both decrease with the reduction of the tilt angle [32]. The JFOM (JFOM = $f_T \cdot V_{BE}$) initially increases and then decreases with the reduction of tilt angle, with the device featuring a 26.6° tilt angle demonstrating the maximum JFOM value of 11.13 THz·V. Through large-signal simulations, the device with optimal tilt angle operating in deep class-AB mode exhibited maximum gain, saturated output power density, and power-added efficiency (PAE) of 12.90 dB, 5.62 W/mm, and 52.56%, respectively [29].

CONCLUSION

This review summarizes the research involving the substrates selection, breakthroughs in epitaxial methods, innovations in doping technology of the GaN material growth technology; and the gate structure design, deposition passivation, and the field plate of the optimazition of GaN HEMT-based devices. These methods can effectively the growth quality of GaN materials and optimize the structure of GaN RF devices, thereby enhancing their performance. Although various research units have successively joined the research and development of GaN RF devices and have made certain research progress, the performance of the device still needs to be improved.At present the quality of GaN crystal growth is facing 3 promblems: (1) lattice mismatch and thermal mismatch (2) Non-uniform doping (3) surface roughness；and the optimazition of GaN HEMT-based devices is facing 4 promblems: (1) short channel effeccts (2) current collapse (3) gate leakage current (4) reduction in breakdown voltage .In the future, the device performance can be further increased through the following aspects: (1) by using the superlattice or nanostructured buffer layers (e.g., AlN/GaN superlattices) to reduce defect density.(2)Using intermediate layer to address the problem of non-uniform doping (3) By controlling temperature, pressure, and the duration of TMGa introduction during the doping process to reduce surface roughness (4) Increasing the aspect ratio and enhancing the confinement characteristics of the two-dimensional electron gas (2DEG) in the channel to suppress the short-channel efffect.(5)Proposing dielectric material deposition methods such as ICP-CVD and Cat-CVD to further enhance device characteristics (6) Using three-dimensional device architectures (e.g., FinFETs, nanowire structures) to enhance gate control. (7) Using the field plate structures and novel micro-tapered gate field plate architecture to enhance device breakdown voltage. Through the joint efforts of researchers, the performance of GaN RF devices will be further advanced.

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